ON THE ESTIMATION OF SWITCHING LOSS IN WIDE BAND-GAP POWER ELECTRONICS SYSTEMS

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ABSTRACT

Switching losses are a central factor in determining the overall performance of modern power electronics applications. It is crucial to accurately and efficiently estimate these losses since they affect system efficiency and power density. Despite the importance of accurate estimations, there is a lack of a broadly-accepted uniform approach for estimating this important loss mechanism across different semiconductor types, ratings, and vendors which limits the ability of engineers to manage the trade-offs inherent in the design of power electronics.

This thesis compares two of the most widely used techniques for estimating switching losses of power semiconductors: continuous converter operation (CCO) and double-pulse testing (DPT). These techniques are evaluated in terms of accuracy, ease of implementation, and metrology considerations. An empirical setup was fabricated to test both techniques on the same platform with minimal changes to the setup between the tests. The same semiconductor was evaluated with both techniques, and the resulting switching loss estimations were then compared. It was found that the CCO technique over-estimates the DUT switching losses by 27.8% on average. This error can likely be attributed to the frequency-dependent losses of the diode, inductor core losses, and the temperature dependence of components. Better agreement between CCO and DPT loss predictions are demonstrated when the frequency-dependent loss of the diode are added to the DPT estimation. This indicates that the CCO method includes additional loss mechanisms and suggests that the results from the DPT technique provide a more accurate estimate of DUT switching losses.

LIST OF ABBREVIATIONS AND SYMBOLS

BJT	Bipolar Junction Transistor
BW	Bandwidth
CCO	Continuous Converter Operation
DMM	Digital Multimeter
DPT	Double-Pulse Test
DUT	Device Under Test
EMF	Electromotive Force
EMI	Electromagnetic Interference
ESL	Equivalent Series Inductance
EV	Electric Vehicle
GaN	Gallium Nitride
HEV	Hybrid Electric Vehicle
HVAC	Heating, Ventilation, and Air Conditioning
ICE	Internal Combustion Engine
IGBT	Insulated-Gate Bipolar Transistor
IT	Information Technology
MCPM	Multi-Chip Power Module
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PQA	Power Quality Analyzer

PSU	Power Supply Unit
Si	Silicon
SiC	Silicon-Carbide
SRF	Self-Resonant Frequency
UPS	Uninterruptible Power Supply
WBG	Wide Band-gap

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CHAPTER 1:

INTRODUCTION

Power electronics are the foundation for many applications that require electrical energy conversion. Currently, electrical loads account for approximately 40% of primary energy consumption in the United States, and estimations project this number to increase worldwide to 50% in the next 25 years [1]. By 2030, as much as 80% of this electric power will use power electronics somewhere in the process of delivering energy to a load [2]. These electronics use switching technology to redirect the energy flow through a circuit many times per second allowing for precise control of the output to a load. The applications of power electronics can range from converters with power ratings in the tens of watts such as consumer laptop chargers to grid level integration systems requiring megawatts of power. Regardless of the application, all power electronics feature a similar goal: to facilitate the transfer of conditioned power from a source to a load.

Although power electronic circuits rely on the switching technology to redirect energy flow appropriately, these same electronics require additional components such as controllers and magnetics to work seamlessly with the switching technology. Power electronics provide a focal point for controls and energy systems to combine [3]. These systems are expected to work continuously over the course of many years, so the many sub-systems must work together effectively with reliabilities approaching 100% [3]. This combination of requirements poses significant challenges for system designers.

1.1. Applications of Power Electronics

Power electronics are used in a variety of applications ranging from low-power consumer devices to high-power grid converters. Figure 1 shows the power levels of some common higher power applications that require power electronics. This section will discuss some of these applications and why power electronics are preferred over alternative schemes.

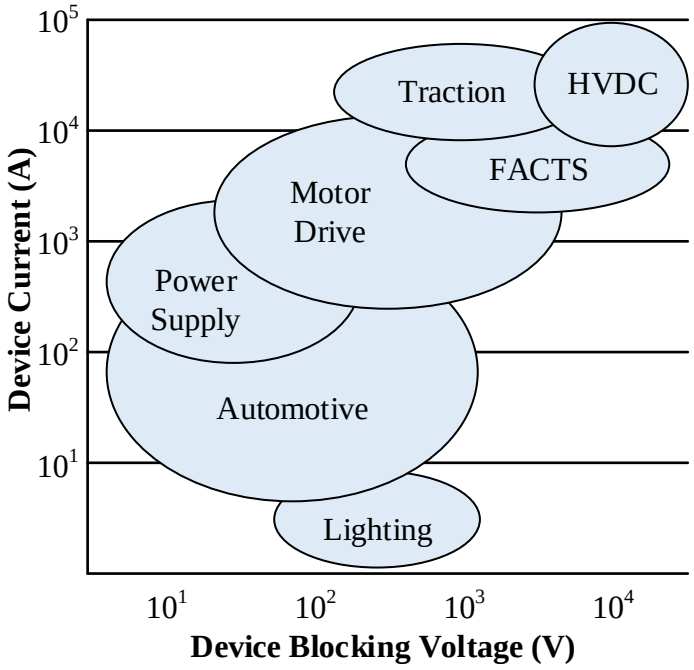


Figure 1: Power levels of various power electronics applications [1]

1.1.1. Electric Motors

Electric motors span across a wide range of applications including compressors, pumps, and fans, and are therefore the largest consumer of electricity by a significant margin [4]. Figure 2 shows two estimations from different sources that indicate the percent of electricity used in the United States by different sectors [4]-[5]. Since heating, ventilating, and air conditioning (HVAC) systems require motors, both estimations shown in Figure 2 predict that motors account for about one-half to two-thirds of the electricity usage in the U.S. Most motor systems have traditionally operated at a constant speed and regulated the load by employing mechanical bleed

valves [5]. Although this operation is effective at controlling the flow rate, it wastes energy since the pump is operating at a faster speed than is necessary. A more effective solution for regulating the flow rate is to use power electronics to control the motor's speed directly and therefore, reduce the wasted energy of the system. It has been determined that switching to electric heat pumps in homes can reduce the energy consumption by as much as 30% and similar advancements are possible in other types of motor systems [5].

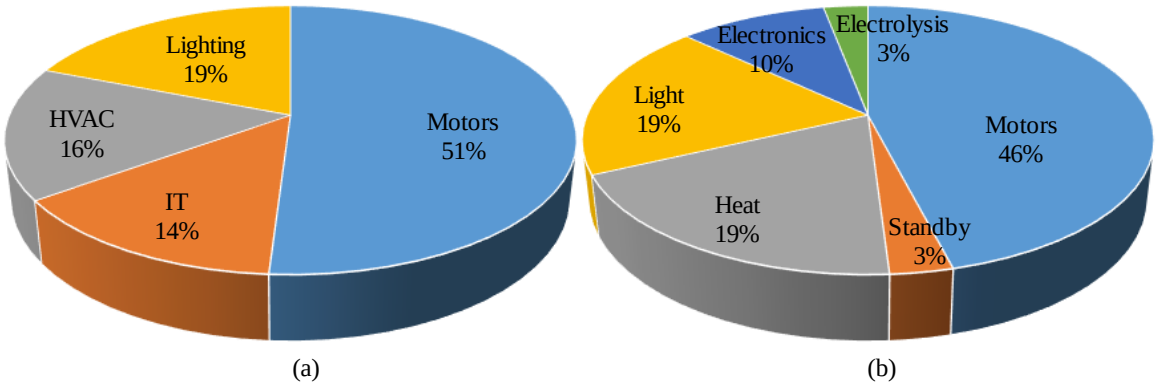


Figure 2: Estimations of electricity usage in the U.S.: (a) [5] and (b) [4]

1.1.2. Renewable Energy

Due to the rising carbon dioxide emissions and increasing demand for electrical energy across the world, several countries are making paradigm shifts from fossil fuels to renewable energy sources such as wind, solar, and hydropower [6]-[7]. By 2020, Europe is expected to use renewable energy sources for 20% of its power generation [6]. Renewable energy sources also offer the opportunity for providing power to remote areas of the world which previously struggled to implement power delivery due to availability, reliability, and cost concerns [8]-[9]. This shift will require a network of hundreds of thousands to millions of power converters linked between the individual renewable energy sources and the remainder of the electrical grid [10]-[11]. Each of these sources will require converters with advanced power electronics to ensure the renewables have an efficient, steady, and reliable interface with the grid [12].

1.1.3. Automotive Powertrains

Several trends are leading to the adoption of electric vehicles (EVs) and hybrid electric vehicles (HEVs). First, carbon dioxide is a negative byproduct of the combustion process in the internal combustion engines (ICEs) typically found in automobiles. Because of the number of automobiles on the roads, the transportation sector now accounts for a large share of carbon dioxide emissions in the world as shown in Figure 3 [13]. Transitioning from ICE cars to EVs and HEVs reduces the carbon diode emissions from automobiles. Second, cars with ICEs rely on fossil fuels, which are a diminishing and non-renewable resource. Governing bodies in many countries are requiring automobiles to use less fossil fuels by increasing fuel efficiency requirements [14]-[15]. For years, automotive manufacturers have been passing these regulations by improving the combustion process in ICE cars, but tightening regulations are forcing manufacturers to produce more EVs and HEVs, which have significantly better fuel efficiency. Third, electric vehicles have a better torque-vs.-power curve for automotive applications, which leads to improved powertrain performance [13], [16].

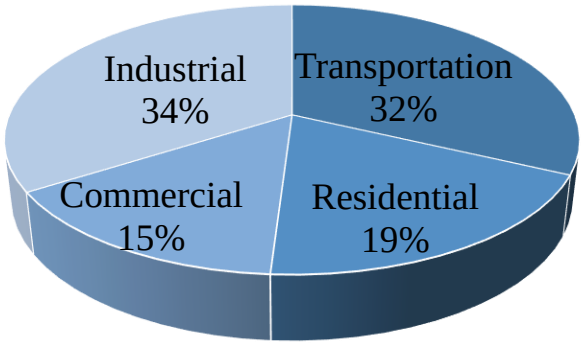


Figure 3: Carbon dioxide emissions distribution [13].

Every EV and HEV requires power electronics to operate the many systems of the automobile such as the propulsion equipment, HVAC, and battery charging system. If these power electronics are physically large or heavy, it reduces the size of the passenger compartment

in the vehicle and reduces the maximum range of the vehicle [17]. Both of these are important performance metrics for a typical automobile. Thus, the automotive industry demands power electronics with high power ratings as well as physically small dimensions and mass for such systems.

1.1.4. Uninterruptible Power Supplies

As stated previously in the Renewable Energy section, the grid is transitioning from centralized power generation to a distributed network of power sources, which all must interface seamlessly. Along with the added penetration of these converters, power electronics in the form of uninterruptable power supplies (UPSs) are being added to the grid. UPSs ensure continuous, high-quality power to critical loads during sags, spikes, or frequency variations in the grid. As information-technology (IT) related business continues to expand and grow, more UPSs are expected to be added to the grid to combat issues with the grid power quality [18]. These devices have a line frequency input and output and must respond nearly instantaneously to perturbations so that the attached loads do not experience these grid quality issues.

1.2. Performance Metrics for Power Electronics

All the applications listed in the Applications of Power Electronics section require high reliability, high efficiency, and quick response time to any shifts in load demand. The strict demands on the power electronics in these applications and many others require metrics to evaluate the performance of power electronic systems. As in many industries, power electronics designers must balance many constraints and trade-offs when designing a product. This section outlines some of the performance metrics used to evaluate power electronics systems.

1.2.1. Efficiency

The efficiency of power electronics gives information as to how much of a converter's power is wasted as heat compared to being passed to the load; this metric relates the input and output power and is defined in Equation (1) [5]:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (1)$$

where P_{OUT} is the converter's output power (also referred to as the converter's rated power), P_{IN} is the converter's input power, P_{LOSS} is the power lost as heat by the converter, and η is the efficiency of the converter. An ideal converter, which cannot be realized in practice, would have no power losses and therefore an efficiency of unity. Practical power electronics applications are now being developed which achieve efficiency values in the range of 98-99% [19]-[21]

1.2.2. Volumetric Power Density

Volumetric power density provides insight into the size of the power electronics with respect to the rated power. This metric is preferred over simply comparing dimensions since, generally, converter volume increases at higher power levels. Power density therefore provides a tool to compare converters even when they have different output power ratings and is defined in Equation (2) [22]:

$$\rho_{vol} = \frac{P_{OUT}}{Vol}\left[\frac{W}{l}\right] \quad (2)$$

where Vol is the converter's volume (including the thermal management solution and any filters) and ρ is the converter's power density expressed in Watts per liter. One well-known method for increasing volumetric power density is to operate a given converter at elevated switching frequency, which enables a significant reduction in the volume of magnetics and energy-storage elements in the system [22]-[23].

1.2.3. Gravimetric Power Density

Gravimetric power density relates a system's output power to its mass. This metric is not often used when evaluating a system installed in a fixed location, but is an essential tool when evaluating transportation systems such as vehicles and aircraft. In transportation applications, mass directly affects the overall system's fuel efficiency, so designs of these systems need converters with very high gravimetric power density [24]. Gravimetric power density, or specific power, is defined in Equation (3) [22]:

$$\rho_{grav} = \frac{P_{OUT}}{Mass} \left[\frac{W}{kg}\right] \tag{3}$$

where $Mass$ refers to the total converter mass including any thermal management solutions and filters. Gravimetric power density can be expressed in Watts per kilogram. Similar to volumetric power density, this metric can be improved by operating converters at elevated switching frequency in order to reduce the weight of magnetics and filter components.

1.3. Estimation of Switching Losses

Owing to the critical role of switching losses in the efficiency-vs.-volume trade-off, the estimation of these losses is of paramount importance during application design. The switching loss of a converter directly affects its volumetric power density, specific power, and efficiency. Therefore, it is one of the most important metrics when evaluating a semiconductor for potential use in any power electronics application design. Despite the importance of estimating switching losses, no standardized technique has been adopted in the literature for this purpose. There are multiple methods used in the literature to estimate switching losses. These techniques can be broadly split into two categories: techniques that estimate the losses using an application circuit and methods that use purpose-built test equipment. This section gives a brief overview of the common switching loss estimation techniques.

1.3.1. Application Based Techniques

These techniques use a device operating as a full converter, often running continuously at the expected operating load and for extended periods of time. These solutions have the advantage of monitoring how the device will operate in an actual application circuit, but it is often difficult to extract the losses specifically due to the semiconductor when using these techniques.

1.3.1.1. Continuous Converter Operation

The continuous converter operation (CCO) technique analyzes a full converter operating at load across a wide range of switching frequencies. By accurately measuring the input and output current while the converter is operating, the power loss at each operating frequency can be calculated. The converter is usually swept across a range of switching frequencies, and the variation of loss with frequency is utilized to isolate the frequency-dependent losses which are assumed to only come from the power semiconductor under evaluation. However, there are some challenges with this technique. First, a full converter with a thermal management solution must be realized before performing this analysis. Second, it is challenging to perform accurate measurements in the system when the converter is operating at full load. Third, it is difficult to isolate only the frequency dependent losses of the device under test (DUT) without including any conduction losses or other frequency dependent losses.

1.3.1.2. Thermal or Calorimetric Methods

These techniques involve measuring the variation of enthalpy of the coolant in a thermal exchanger that is used to cool the semiconductor devices in a converter [25]. The heat dissipated by the DUT is measured, and since the device is operating continuously, the measurements can be slow [26]. The challenges with this technique are similar to the CCO case in that it is difficult to isolate only the losses of the DUT due to switching. The thermal measurements include both

conduction losses and switching losses, so this method requires an accurate understanding of the DUT's conduction losses to estimate switching losses. In addition, these thermal measurements generally include losses from any auxiliary circuitry in the system. These auxiliary circuits also participate in heating the thermal exchanger, so their losses must be subtracted to isolate the contribution of the DUT [27]. Finally, this technique requires repeated calibration of the setup and is often only tuned to operate across a small range of output power levels.

1.3.2. Purpose-Built Equipment Techniques

The second main category of techniques require purpose-built metrology to estimate the switching losses of a DUT. In general, the circuits used in these procedures are not representative of an actual application circuit, but are designed specifically to permit isolation of the DUT losses across a range of operating conditions.

1.3.2.1. Opposition Method

This technique uses two converters attached to the same input voltage and operating with opposite energy transfer directions [28]. One converter operates as a generator and the second converter operates as a receptor, with high power circulating through the two converters [25]. The main advantages of this technique are that the measurements introduced into the system are non-intrusive and no dissipative load is added to the system. The disadvantages of this technique are that losses are not evaluated directly across the DUT, so other losses must be removed from the measurements in order to accurately estimate the DUT switching loss [29].

1.3.2.2. Double-Pulse Test

The double-pulse test (DPT) technique uses time-domain measurements of turn-on and turn-off switch transitions to estimate the switching losses of the DUT [30]. The DUT is attached to a specialized test circuit that facilitates the precise selection of specific operating conditions

during a very brief transient operation period. This technique does not require any thermal management solution since the device is only operated for a brief period. This technique also provides isolation of the DUT losses because measurements are applied directly to the terminals of the DUT. The main challenge with this technique is the difficulty in making sufficiently accurate measurements to reliably compute the DUT losses from the captured transient waveforms.

1.4. Thesis Objective

In light of the central role of switching losses in determining the overall performance of modern power electronics applications, the ability to estimate these losses accurately and efficiently is crucial. The lack of a broadly-accepted uniform approach for estimating this important loss mechanism across different semiconductor types, ratings, and vendors limits the ability of engineers to manage the trade-offs inherent in the design of power electronics. To address this limitation, this thesis provides a detailed analysis of the two most widely used techniques for estimating switching losses of power semiconductors: CCO and DPT. As part of this analysis, the two techniques are compared against one another in terms of their accuracy, ease of implementation, and metrology requirements. This study concludes with a set of specific recommendations to assist power electronic system designers in properly estimating switching losses for the purpose of application optimization.

1.5. Thesis Organization

This thesis is organized into seven chapters. Chapter 2 provides background information on the reason switching losses exist and describes the type of semiconductor evaluated in this thesis. Chapter 3 and Chapter 4 go into more detail about the CCO and DPT switching loss estimation techniques, respectively. These two techniques are evaluated over the other loss

techniques since they use similar components and are commonly reported in the literature. Chapter 5 introduces the empirical platform used to compare the two switching techniques. Chapter 6 presents the results of this comparison and provides an associated analysis. Finally, Chapter 7 provides concluding remarks and discusses future extensions of this work.

CHAPTER 2:

BACKGROUND

Traditionally, the limiting factor for achieving higher efficiency and power densities in power electronics has been the semiconductor. In the last decade, wide band-gap (WBG) semiconductors have emerged as an alternative to conventional silicon (Si) semiconductors by offering improvements to some of the known limitations of Si devices. WBG devices are capable of faster edge rates which can significantly reduce system losses. This chapter outlines the motivation for the shift in power electronics to WBG technology and details some of the challenges associated with integrating and measuring WBG semiconductors.

2.1. Traditional Power Semiconductors

Ideally, the switching in power electronics would be performed with a switch that changes state instantaneously, conducts current without any losses while in the on-state, and blocks voltage with no leakage while in the off-state. However, since this ideal switch cannot be realized in practice, a variety of competing semiconductor technologies have emerged, each of which has distinct advantages and disadvantages. Figure 4 presents the power and frequency ranges supported by each of the major silicon semiconductor types used today. The focus of this thesis is power levels above a few hundred Watts and switching frequencies above 1 kHz. Traditionally, only insulated-gate bipolar transistors (IGBTs) are able to operate at these levels. However, even IGBTs cannot reach potential applications in the high-frequency, high-power regions that are missing in Figure 4.

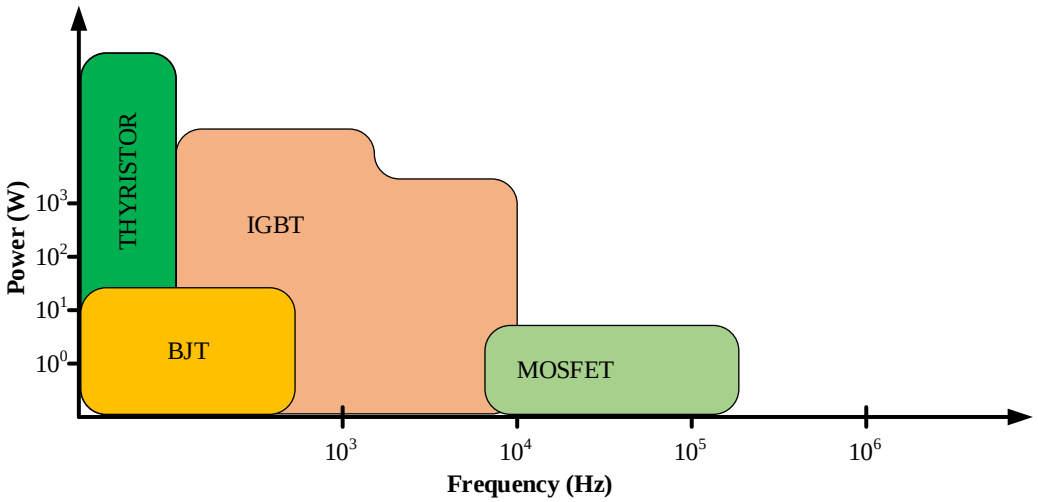


Figure 4: Power & frequency relationship of Si semiconductors [31].

2.2. Wide Band-Gap Semiconductors

Many applications need semiconductors that can operate in this untapped space. Accordingly, new semiconductor technologies have been proposed to address these missing regions and challenge silicon technology in the regions already covered. The most prominent of these alternatives are WBG devices; Figure 5 shows the power and frequency relationship plot with two WBG technologies added to the plot: gallium nitride (GaN) and silicon carbide (SiC).

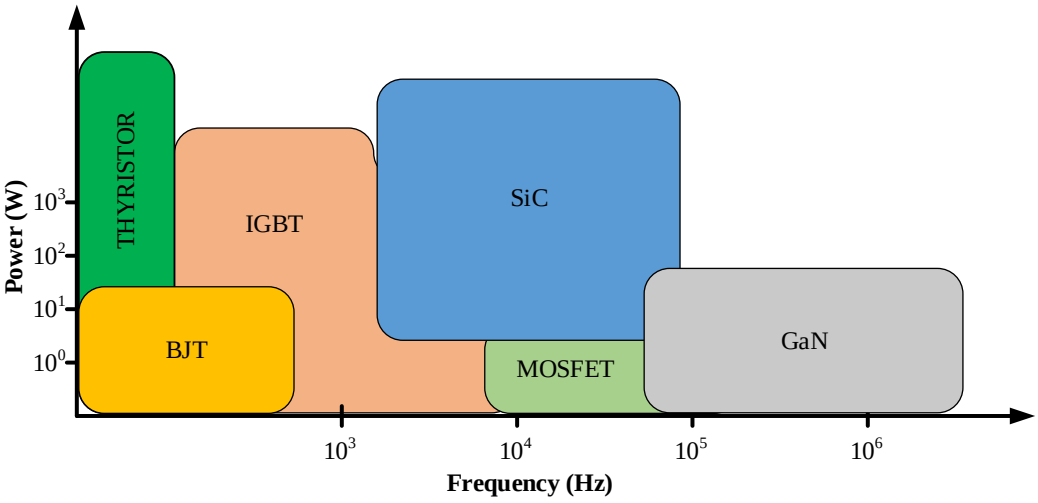


Figure 5: Power & frequency relationship including WBG [31].

Due to the power levels targeted in this thesis, only SiC devices will be evaluated in detail. As shown in Figure 5, SiC devices are able to operate at higher power and frequency levels than Si IGBTs. In addition to these improvements, SiC semiconductors have higher blocking voltage ratings, operating temperatures, and lower switching losses than Si IGBTs. To illustrate this important property of WBG devices, the switching loss for a Si IGBT and a SiC MOSFET with nearly identical ratings are compared in Figure 6 [32]-[33].

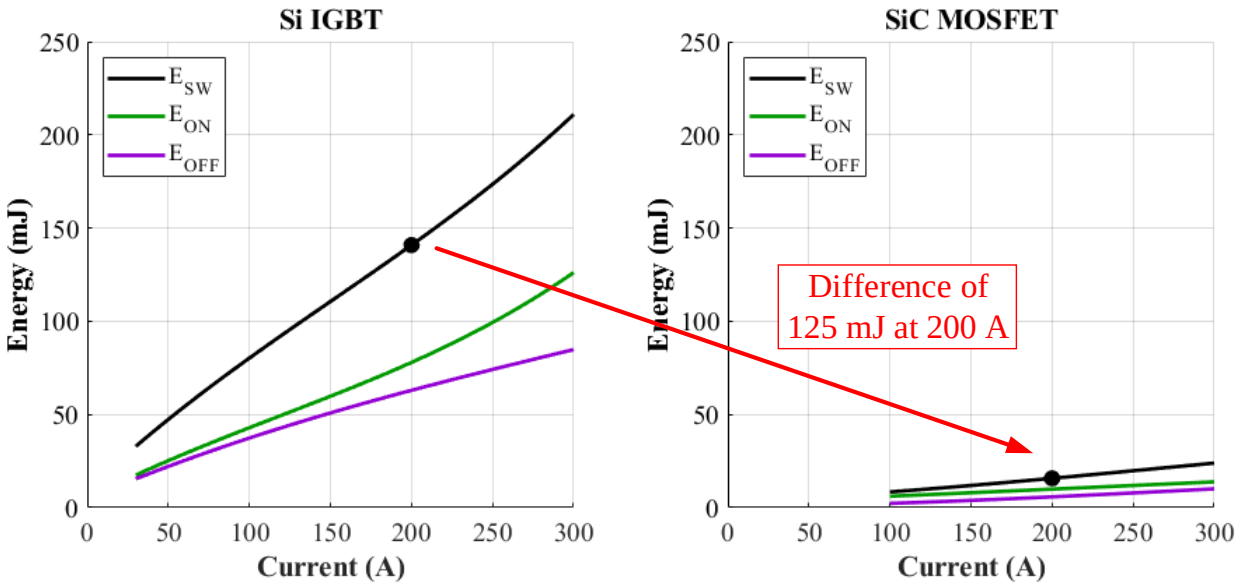


Figure 6: Switching loss comparison of (a) Si IGBT [32] and (b) SiC MOSFET [33]

As illustrated in Figure 6, the switching loss of the SiC MOSFET is 125 mJ lower than the switching loss of the Si device when operating at 200 A. If both devices are operated in a hard-switched application at 1 kHz, using the SiC device instead of the Si devices produces a switching power reduction of 125 W. Although there are additional advantages to transitioning to WBG devices, this thesis will focus on the advantage associated with reduced switching loss.

2.3. Understanding Switching Losses

To understand the advantage associated with reduced switching loss, it is first important to understand why switching loss occurs. This section outlines this foundation and then details the reasons that SiC semiconductors have lower switching loss than Si semiconductors.

2.3.1. Switching Losses

During the transition from the on-state to the off-state or vice-versa, there is a period of time during which the device is conducting current while a voltage is expressed across its terminals. During these overlap periods, the device experiences switching loss. Figure 7 shows a notional representation of these current and voltage overlap periods along with the corresponding instantaneous power loss during these switching events.

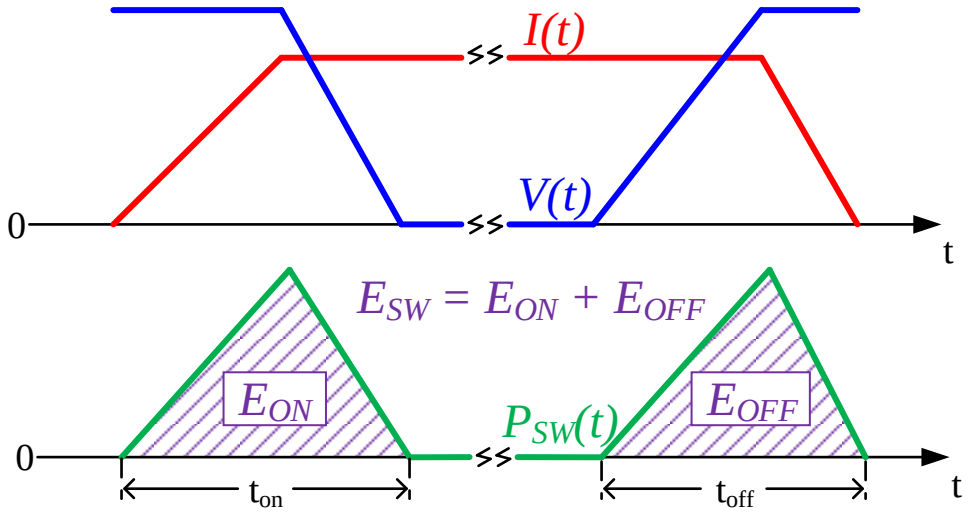


Figure 7: Notional representation of the switching loss [5]

The instantaneous power during the transitions is calculated by multiplying the instantaneous voltage and current at each point as shown in Equation (4). This instantaneous power metric by itself does not provide much insight into the semiconductor's losses in an application since it only states the power being dissipated at a particular instant. A more useful

metric is the switching energy, which is calculated by integrating the instantaneous power waveform over one period as shown in Equation (5):

$$P_{SW}(t) = v(t) \cdot i(t) \tag{4}$$

$$E_{SW}(t) = \int_{T_s} P_{SW} dt = \int_{T_s} v(t) \cdot i(t) dt \tag{5}$$

where $v(t)$ is the time-dependent voltage across the semiconductor, $i(t)$ is the time-dependent current through the semiconductor, P_{SW} is the time-dependent power dissipated by the semiconductor, T_S is the switching period, and E_{SW} is the total energy consumed due to switching. This energy value is useful because it gives a metric that offers insight into the average power the semiconductor will dissipate while operating in an application. This energy value can be multiplied by a converter's switching frequency to determine the average power loss in the semiconductor due to switching. This relationship is described by Equation (6):

$$\overline{P_{LOSS,SW}} = f_s \cdot E_{SW}(t) \tag{6}$$

where $\overline{P_{LOSS,SW}}$ is the average power loss in a given semiconductor device due to switching. If the device switching energy is known with high fidelity, Equation (6) can aid in selecting an optimized switching frequency for a given application.

In many applications, it is useful to split the total switching loss into the two independent switch transitions, turn-on and turn-off. The independent ON and OFF energies can be determined by separately integrating the instantaneous power over the turn-on time (t_{on}) and the turn-off time (t_{off}). These integrations along with their relation to the total switching loss are presented in Equation (7):

$$E_{SW}(t) = E_{ON}(t) + E_{OFF}(t) = \int_{t_{on}} P_{SW} dt + \int_{t_{off}} P_{SW} dt \tag{7}$$

where $E_{ON}(t)$ is the switching loss due to the turn-on process and $E_{OFF}(t)$ is the switching loss due to the turn-off process.

Analysis of these equations along with Figure 7 reveals that there are four ways to decrease semiconductor switching loss: (1) reduce the operating voltage, (2) reduce the operating current, (3) reduce the converter switching frequency, or (4) reduce the voltage and current overlap time. The effect of options (1), (2), and (4) on the power loss is illustrated in Figure 8. The impact of a reduced switching frequency is not shown in the figure since only one switching period is shown. However, this mechanism would result in fewer instantaneous power spikes for an equivalent amount of time.

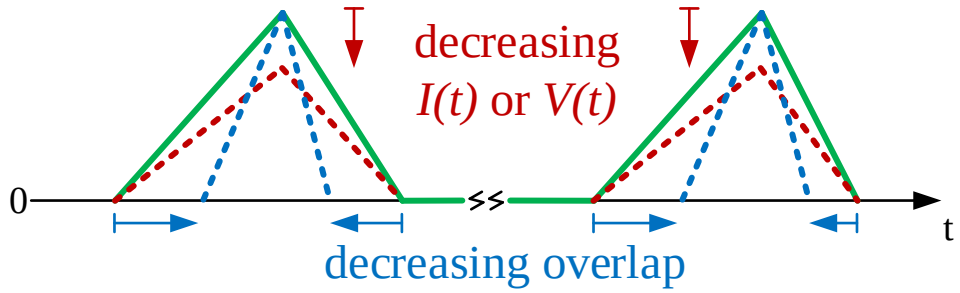


Figure 8: Impact of various techniques to decrease switching loss in semiconductors

While decreasing the bus voltage or operating current successfully reduces switching losses, both options degrade the output power for the system and therefore lower its power density. In addition, in many topologies, the voltage and current operating levels are dictated by the requirements of the load and cannot be adjusted. The third option, decreasing the switching frequency, would require larger passive components to store more energy over the lengthened switching period. This would also negatively impact power density. Therefore, the fourth technique, reducing the voltage and current overlap time, is the most attractive option. This is achieved by increasing edge rates during the turn-on and turn-off transitions.

2.3.2. Edge Rates

To understand why different semiconductor devices have varying edge rates, one must understand the influence of parasitics on device performance. All semiconductor devices have intrinsic capacitances due to their internal structure. In addition, all semiconductors have interconnect inductance due to the device packaging and layout. These parasitic elements are shown for a MOSFET in Figure 9.

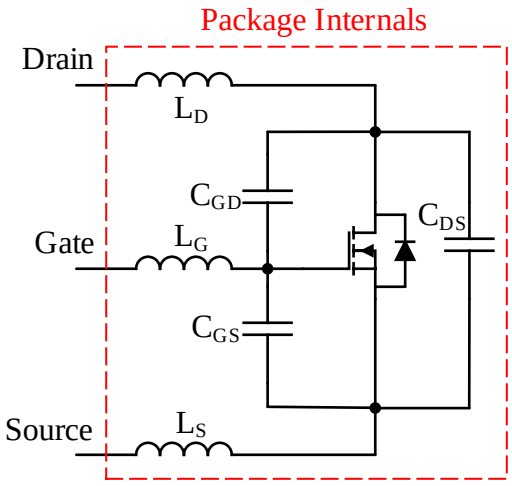


Figure 9: MOSFET parasitic elements

During switching transitions, the intrinsic capacitances of the semiconductor device must be charged or discharged before the switching event completes. These capacitances are the main reason for the non-instantaneous nature of switching transitions. Reducing the device intrinsic capacitances increases the maximum attainable device edge rates and therefore lowers switching losses. Compared with Si devices, SiC semiconductors have significantly smaller intrinsic capacitances [34].

Edge rates and switching frequency are related, but not the same. In order to achieve high switching frequencies, a semiconductor must support fast edge rates, but fast edge rates do not mean that the device must be operated at high frequencies. This relationship is due to the

transient thermal behavior of the semiconductor device. During a switching event, a device heats up very quickly due to switching loss. To prevent thermal runaway, the device must have sufficient time to cool before the next transition causes additional heat generation. Dodge and Hess suggest that the total transition time ($t_{on} + t_{off}$) should not exceed 5% of the switching period to prevent thermal runaway in most applications [35]. From this analysis, it is seen that in addition to reducing switching loss, fast edge rates also enable operation at elevated switching frequencies.

2.4. WBG Semiconductors – Practical Considerations

Although the fast edge rates supported by WBG devices allow for decreased switching losses, they also cause some undesired side-effects. The main reason is that the fast edge rates excite resonances among parasitic elements such as those shown in Figure 9. Although these parasitics also exist in Si devices, Si device edge rates are generally too slow to stimulate resonance among these elements. To illustrate the effect of these parastics, Figure 10 shows a comparison of a single turn-off event for a SiC MOSFET and a Si IGBT at identical operating conditions of 600 V and 20 A [36].

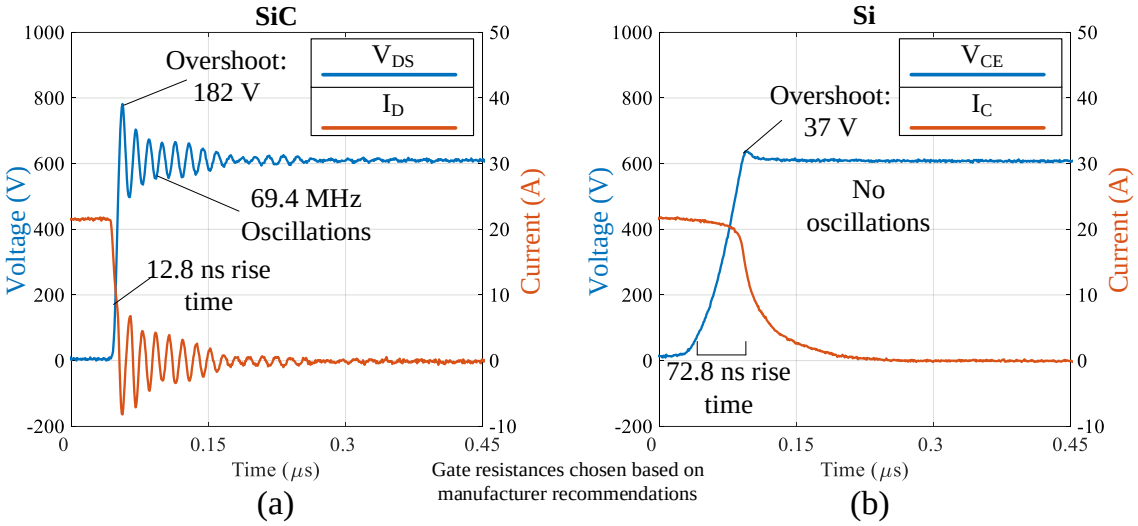


Figure 10: Comparison of turn-off event of (a) SiC MOSFET and (b) Si IGBT [36]

These two devices were selected because they have similar device ratings and would typically compete for the same applications. Before discussing some of the challenges with WBG semiconductors, it is important to first indicate that this plot clearly corroborates the previous claims that WBG devices have faster edge rates than Si devices. In the comparison shown, the voltage rise time of the SiC device is nearly six times faster than the rise time of the silicon device, resulting in a 13x improvement in switching loss.

2.4.1. Overshoot

The high current edge rates of WBG switching events create voltage overshoot due to back electromotive force (EMF) from the parasitic inductances. Similarly, the high voltage edge rates cause large displacement currents through the device intrinsic capacitances. When device edges rates are increased, the overshoot present in the device's voltage and current waveforms also increases. In Figure 10, the voltage overshoot of the SiC device is almost five times the voltage overshoot of the Si device. Although the devices can still operate in these conditions, the increased overshoot potentially degrades the device lifetime and requires increased margins to avoid device failure.

2.4.2. Oscillations

Because resonances among parasitic elements are more likely to be excited by fast edge rates, WBG devices demonstrate increased underdamped ringing after switch transitions compared to Si devices. In Figure 10, the silicon IGBT waveforms demonstrate no oscillation, but the SiC device waveforms demonstrate significant oscillation at nearly 70 MHz. These underdamped oscillations can be problematic as they may cause application circuits to malfunction under certain circumstances. However, this challenge can be addressed in part by

minimizing parasitic elements and by adding dissipative elements to the circuit such as snubbers [37]-[38].

2.4.3. Electromagnetic Interference

WBG systems often exhibit much stronger electromagnetic interference (EMI) signatures than Si-based systems due to increased high-frequency content [39]-[43]. The faster edge rates supported by WBG devices are in part responsible for this increased EMI footprint. This increase in EMI magnitude can be mitigated using traditional EMI filter techniques, although new techniques to address this challenge are also under development [42]. Irrespective of technique, the EMI impact of high edge rates must be considered when using WBG devices for application design.

2.4.4. Metrology Considerations

Elevated edge rates also cause difficulties for performing high-fidelity time-domain measurements of WBG device waveforms. Fast edge rates and high-frequency oscillations increase the bandwidth requirements of the metrology necessary to perform these measurements. This increases both the cost and circuit complexity of available metrology solutions. In addition, the parasitic elements present in the ancillary circuit used to evaluate a semiconductor can substantially influence DUT measurements. The challenges associated with accurately characterizing WBG devices represent the principal motivation for this research. The following chapters discuss two of the primary techniques used to estimate the switching losses of WBG semiconductors.

CHAPTER 3:

CONTINUOUS CONVERTER OPERATION

For laboratories or organizations that do not have access to purpose-built hardware for characterizing semiconductor switching loss, an attractive alternative is to implement and operate a converter for this purpose. By operating the converter across a range of switching frequencies, an estimate for semiconductor switching loss can be determined. This chapter outlines the process of estimating semiconductor switching loss using this method, which will be called continuous converter operation (CCO), and discusses the associated challenges.

3.1. CCO Description

For the continuous converter operation technique, a complete power electronics converter is designed, fabricated, and evaluated. The converter can be operated under open- or closed-loop control; but it must be thermally stable at full load. The switching frequency of the converter is swept across a range of values while operating at load. At each switching frequency, the converter is operated continuously until it reaches both electrical and thermal steady-state. Once in steady-state, the average input and output voltages and currents are measured and used to calculate the average input and output power values. The difference in the input and output power values is used to determine the average power loss at each switching frequency, which is then plotted as a function of frequency [44]-[48]. A notional example of the expected power loss as a function of frequency is provided in Figure 11.

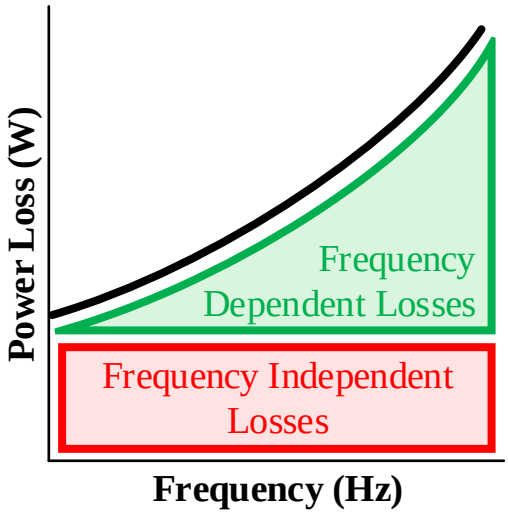


Figure 11: Notional example of power loss versus frequency plot

By observing the slope of the loss-vs.-frequency plot, the switching loss of the DUT can be estimated at each switching frequency considered. Through unit analysis, it can be shown that the slope of the loss-vs.-frequency plot produces a value in Joules, which can be linked to the total per-cycle switching energy associated with operation of the converter. This is demonstrated in Equation (8), where the brackets indicate the units of each parameter.

$$\frac{\Delta P_{LOSS}}{\Delta f_s} \rightarrow \frac{[W]}{[Hz]} = \frac{[J/s]}{[1/s]} = [J] \tag{8}$$

It should be noted that the loss-vs.-frequency plot may or may not be linear for a given converter. The linearity of this plot will be discussed later in this thesis. However, if the results are linear, this analysis produces a single switching loss estimation that can be compared with other loss estimation techniques.

3.2. Advantages of CCO

One significant advantage of the CCO technique is that the metrology is very simple. The necessary current and voltage probes can be attached directly to the terminals of the converter. This method is non-intrusive since no modification must be made to the conduction

paths within the converter. The non-intrusive nature of this technique is contrary to other loss estimation methods that require probes to be attached directly to the DUT terminals. The CCO technique can even be applied to converters for which no information is available about the details of the internal components.

Another presumed advantage of the CCO technique described in the literature is that this technique requires only low-bandwidth instrumentation. While it is true that only low-bandwidth measurements are necessary, it will be shown later in this thesis that there are other challenges associated with CCO metrology, even if the bandwidth requirements are low. Regardless, low-bandwidth metrology is typically less expensive than metrology that can measure high-frequency dynamics.

The final advantage of the CCO technique is that a converter may already be required to fulfill project deliverables. In this case, building a converter for CCO analysis does not add additional steps to the design process. This technique simply uses the resources that are already available once the converter is built.

3.3. CCO Metrology Considerations

The CCO technique relies on several metrology assumptions that must be true for the loss estimations to be accurate. This section first discusses some of the risks associated with making these assumptions and second, details some of the challenges with making high fidelity continuous measurements using a converter at full load.

3.3.1. Separation of Conduction and Switching Losses

The first major assumption of CCO it that frequency-dependent and frequency-independent losses can be separated. This assumed split is shown visually in Figure 11. The validity of this assumption requires that the conduction losses remain constant across all

considered frequencies. If this assumption is false, then the conduction losses must be removed in a more rigorous way than simply subtracting the y-intercept of the plot from the computed total loss value at each frequency. The problem with this assumption is that at different frequencies, components operate at different temperatures. This assumption becomes invalid if any components in the circuit have conduction properties with significant thermal dependence. For any components with this dependence, conduction losses in the circuit will change as a function of frequency due to the varying thermal characteristics. Although these changes are actually variations in conduction losses, they appear in the loss-vs.-frequency plot as frequency dependent losses. For example, some of the known temperature dependent circuit parameters that can affect the switching loss estimation in a boost converter are shown in red in Figure 12.

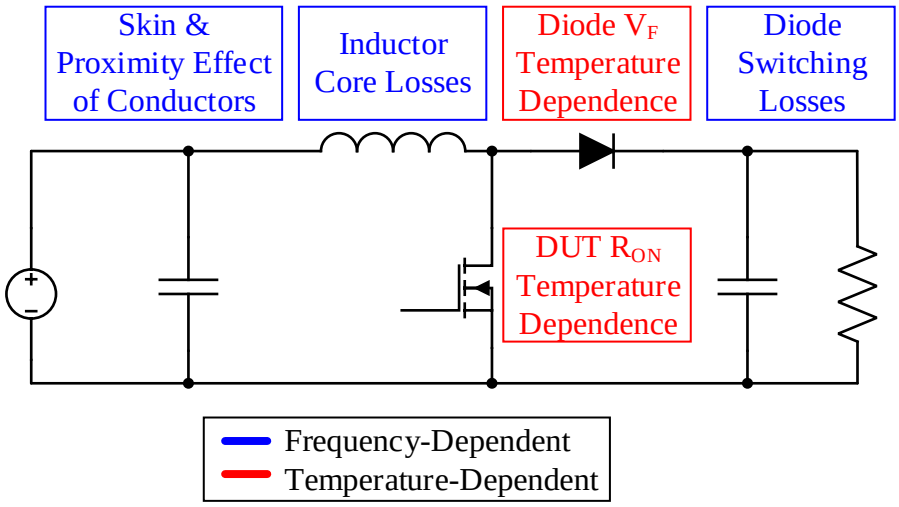


Figure 12: Additional losses in a boost converter

Thermal variation of components has been recognized in the literature as a potential source of error in CCO switching loss estimation [46]-[47]. In these studies, authors have attempted to improve the removal of frequency-independent losses by monitoring the DUT's temperature during converter operation. Conduction losses can then be estimated using the measured temperatures rather than assuming that conduction losses are constant across operating

frequencies [46]-[47]. The challenge with this suggested improvement to CCO is that it requires an accurate thermal model of the semiconductor package and relies on temperature readings that may have limited accuracy. Regardless of the achieved accuracy, these attempts suggest that the temperature dependence of conduction loss may impact the switching loss estimations obtained via CCO. Therefore, for the conventional CCO technique to be accurate, it is important that the temperature dependence is negligible for all circuit elements in the system under study.

3.3.2. Frequency Dependent Losses in Ancillary Circuit Components

Using the slope of the loss-vs.-frequency plot to estimate switching losses assumes that the semiconductor under consideration is responsible for all of the frequency-dependent losses in the system. If any other frequency-dependent loss mechanisms in the circuit cannot be ignored, then this estimation technique over-predicts the losses due to the semiconductor. Some of the notable frequency dependent losses that may exist in a converter include diode reverse recovery losses, diode capacitive losses, inductor core losses, and high-frequency ohmic losses due to skin and proximity effect. Some of these frequency-dependent losses are shown in blue in Figure 12.

Some researchers have identified this assumption as a potential concern and have described advances to the CCO technique to try to address it. For example, Saito et al. claim that the switching losses of the diode cannot be neglected and attribute the frequency-dependent losses measured through CCO to be the combination of DUT losses and diode losses rather than just DUT losses [45]. Similarly, Xia et al. claim that inductor core losses cannot be ignored and attribute the frequency-dependent losses to the combination of the DUT switching losses and the core losses of the inductor [46]. The potential for other frequency dependent losses in the converter is a limitation of the CCO estimation technique.

3.3.3. Linearity of Frequency-Dependent Power Loss

To extract a single switching loss estimation value from the loss-vs.-frequency plot, this relationship must be linear. If non-linear behavior is observed, then the switching loss estimation value is a function of the switching frequency of the converter. While most of the CCO literature assumes that the loss-vs.-frequency plot is linear, this may not be the case when non-linear factors such as core losses are considered. A thorough treatment of the linearity of the loss-vs.-frequency plot can be found in [49].

3.3.4. Challenges with Accurate Current Measurement

The final metrology consideration for CCO involves the measurement instrumentation instead of the loss estimation process. Although the metrology requirements for CCO are modest in terms of sensor and instrument bandwidth, the converter is operating at full load while the associated experiments are performed. This produces challenges due to the thermal characteristics of the metrology equipment considered, and especially for the current measurements. This behavior is best understood through an example. To demonstrate this concept, a power supply unit (PSU) with integrated current measurement was attached in series with a precision current shunt, a power quality analyzer (PQA) configured to measure current, and an oscilloscope current probe [50], [51]. The PSU was configured for current-mode control, and no load was attached between the PSU terminals other than the current sensors. A schematic diagram of this test circuit is shown in Figure 13.

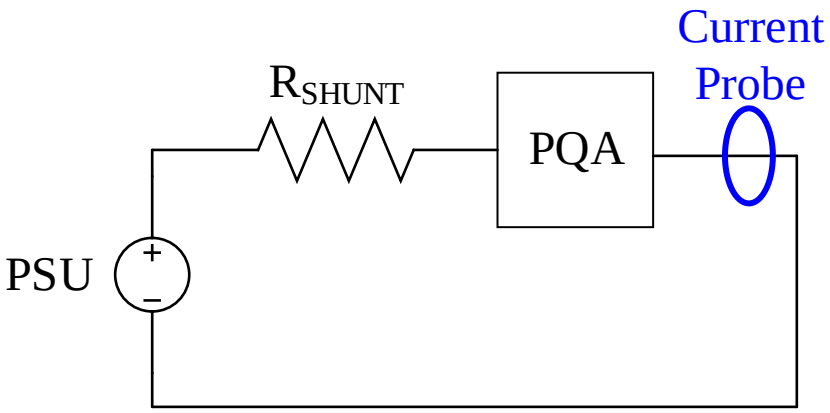


Figure 13: Low bandwidth current measuring test circuit

For this analysis, the PSU current set-point was swept from 8 to 26 A in 2 A increments. At each operating current, measurements were recorded from all the three instruments – the current shunt, the PQA, and the current probe – after the setup stabilized for five minutes at the selected operating current set-point. The percent difference of each instrument reading with respect to the configured PSU current is shown in Figure 14.

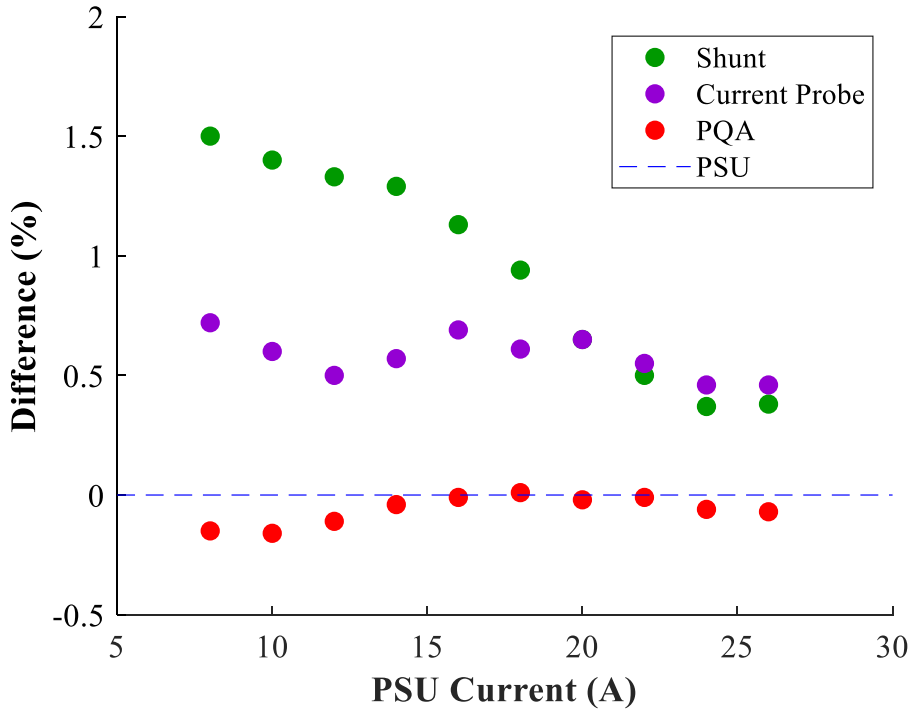


Figure 14: Percent difference of current measuring instruments with respect to PSU

Although all three current sensors in this setup are expected to report the same value, it is clear that there are some systematic differences in the measurement results. This analysis does not assume that the PSU's current measurement is the most accurate of the considered sensors. This plot simply illustrates that commonly used current sensors may report different values when measuring the same current. These discrepancies may manifest as an offset, such as the difference between the PQA and the current probe in Figure 14. These discrepancies may also manifest as a scale factor, such as the difference between the current shunt and the PQA in Figure 14. For the purposes of this plot, any of the measurement techniques could have been used as the reference.

An additional challenge of the CCO technique is that, while the bandwidth requirements of the metrology are low, there is still high-frequency content present in the measured signals. Digital multimeters (DMMs) often perform some level of signal conditioning when making dc voltage measurements. The presence of this high-frequency content in the converter can influence the multimeter's signal conditioning, which causes the displayed measurements to be inaccurate. It has been suggested that the switching loss estimated from CCO can include error greater than 10% if poor metrology is used, and that this error can be as low as 0.1-1% when high-accuracy metrology is used [25]. The outcome of this analysis suggests that even though CCO uses low-bandwidth measurements, the metrology must still be carefully considered when applying this technique.

3.4. CCO Circuit Considerations

The major challenges with the CCO circuit stem from the necessity of designing and building a complete converter for analysis. This technique may require significant design effort to evaluate the switching loss of a new semiconductor device, depending on its ratings and

packaging. This section outlines some of the challenges associated with designing a converter to perform CCO measurements.

3.4.1. Thermal Challenges

For WBG systems, it is typical for discrete semiconductors to be employed in converters that reach power levels in the multiple kilowatt range. Designing a converter that is thermally stable at these power levels becomes a significant challenge. Since the CCO technique requires thermal stability at all switching frequencies considered, the thermal management solution must be sized to account for losses at the upper end of the analysis frequency range, which may be significantly higher than the designed operating frequency of the converter. This may require a large and expensive cooling system that must be closely monitored while operating the converter.

3.4.2. Closed-Loop Operation

Production converters are designed with closed-loop control to handle changes in the load and inconsistencies in the input power. The CCO technique requires that the DUT blocks the same voltage and conducts the same current at all frequencies. Depending on the converter topology, these parameters may not be the same parameters that are regulated by the controller. If the converter is operated with closed-loop control that regulates other parameters, the trends reflected in the loss-vs.-frequency plot may be influenced by changes in the DUT's operating conditions other than switching frequency.

To overcome this potential issue, the CCO technique can be used with an open-loop circuit that is regulated by an operator. This ensures that the DUT is operated at the same operating conditions across all switching frequencies. However, this also increases the time required to implement the CCO technique.

3.4.3. Changing Operating Conditions

Converters are often optimized for specific operating conditions. This presents a challenge when using CCO to understand the sensitivity of switching loss to changes in system parameters. To understand such sensitivities, it may be necessary to operate a given converter at various voltage and current levels. Designing for a range of inputs and outputs adds an additional level of complexity when designing a converter to support CCO analysis procedures.

3.5. CCO Summary

Continuous converter operation analysis can be used as a non-intrusive method to estimate switching loss for active semiconductor devices. However, there are challenges associated with the application of this technique. Specifically, several assumptions are made in the implementation of this technique which may not always be valid. For example, this technique generally assumes that conduction losses are constant across all frequencies and that the DUT's switching loss dominates over all other frequency-dependent losses. In addition, operating the converter at full load requires a robust thermal management solution; and challenges may be experienced with accurately measuring the input and output current of the converter. Despite these challenges, CCO provides a useful way to evaluate DUT switching loss when the necessary conditions can be properly met.

CHAPTER 4:

DOUBLE-PULSE TEST

Rather than designing and implementing a full-converter with a thermal management solution, the other switching loss estimation technique relies on precise measurements of the instantaneous voltage and current during one OFF and one ON transition of a semiconductor. This technique, called the double-pulse test (DPT), provides a snapshot of how the DUT will operate in a full converter, without the design time required to design and build such a system. This chapter details the DPT procedure along with the challenges associated with properly measuring the DUT's dynamics.

4.1. DPT Description

The double-pulse test uses time-domain measurements of turn-on and turn-off transitions to estimate the switching losses of a DUT [52]-[55]. The circuit used for DPT, shown in Figure 15, involves the DUT connected to an inductor and freewheeling diode in parallel.

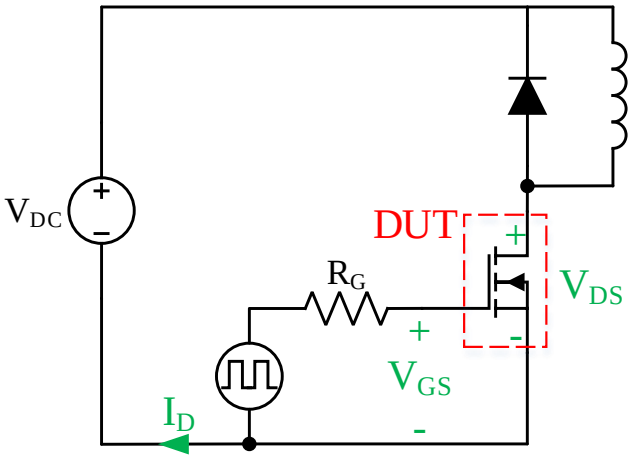


Figure 15: Schematic for double-pulse test

In a DPT, the DUT is turned on twice for different lengths of time. During the first on-time, often referred to as the “charge pulse”, current flows directly from the input power supply through the inductor and the DUT as shown in Figure 16(a). Assuming the inductor is properly designed for a DPT, the inductor current will linearly increase as a function of time during the charge pulse time. When the inductor current reaches the target DUT current level, the device is turned off. During the off time, the current in the inductor continuous to freewheel through the diode as shown in Figure 16(b). The current continues in this loop until the DUT is turned on again. When the DUT is turned back on, the current once again follows the path shown in Figure 16(a).

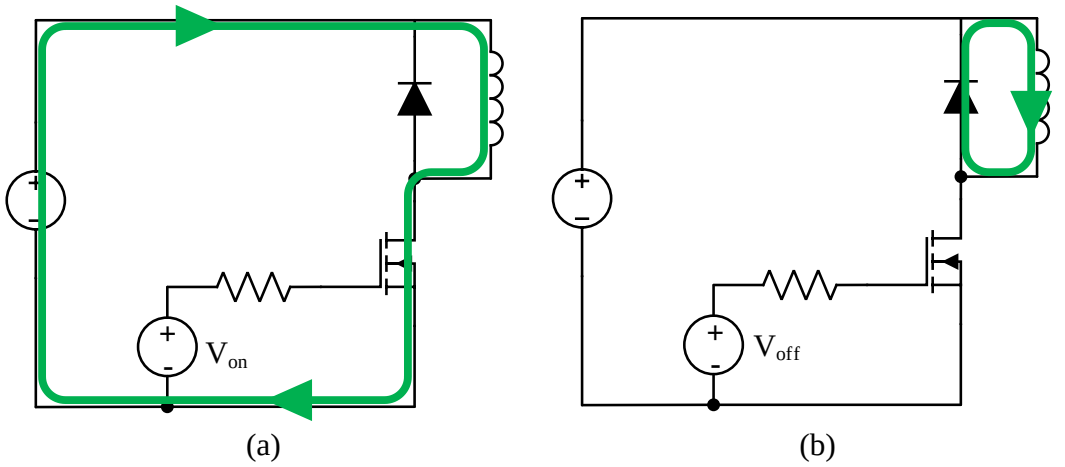


Figure 16: Current flow during DPT (a) on-time and (b) off-time.

A notional diagram of the time-domain waveforms for a DPT sequence is shown in Figure 17. The first subplot, the V_{GS} waveform, represents the control signal for the DUT; a high signal indicates that the device is conducting, and a low signal indicates the DUT is blocking. The second subplot is the drain current through the DUT, annotated I_D; and the third subplot is the drain-to-source voltage across the DUT, annotated V_{DS}. In Figure 17, the first on-pulse is longer than the second on-pulse. This is common in DPT since the length of the first pulse is tuned to charge the inductor to the desired load current value, while the length of the second

pulse must only be long enough to ensure the switching dynamics have settled. The diagram indicates two important characteristics of the DUT's current and voltage characteristics. First, while the DUT is conducting, the drain current waveform has a linear slope as the inductor is charged. Second, while the DUT is off, it blocks the entire input bus voltage. These observations highlight one of the advantages of DPT: the exact DUT voltage and current operating conditions can be precisely controlled by simply adjusting the input dc voltage and varying the length of the charge pulse to reach a target current based on the inductor ramp time. This observation, while subtle, allows for easy manipulation of the DUT's operating conditions to predict losses across a range of operating conditions.

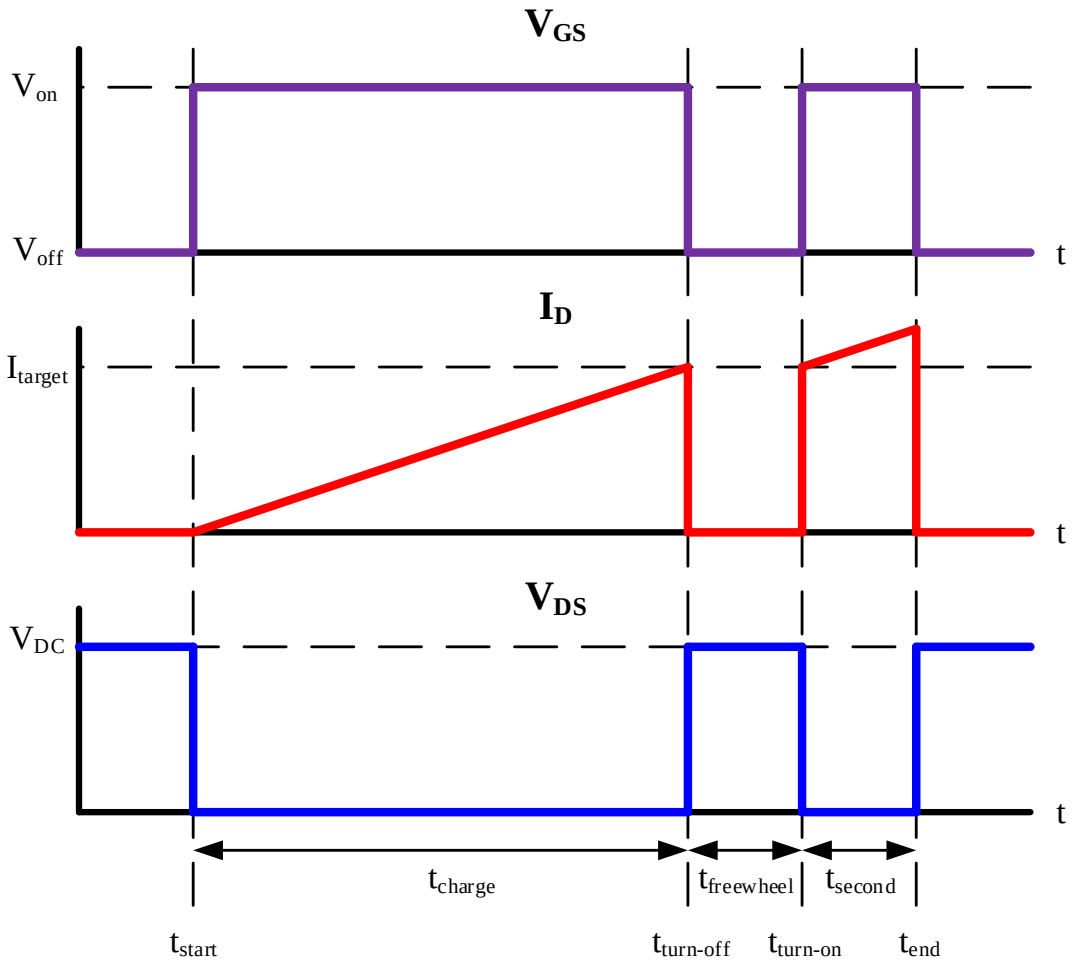


Figure 17: Notional DPT waveforms

In a DPT, there are two transitions that are of primary interest: (1) the turn-off event at the end of the charge pulse, and (2) the turn-on event at the start of the second on-pulse. These two transitions are highlighted in Figure 18 and are important because they occur at nearly the same operating conditions. The only difference in the operating conditions of these two transitions results from the losses that occur in the inductor and diode during the freewheeling off-time; these losses are generally negligible. These two important transitions provide a snapshot of the DUT's dynamic behavior over one period of a converter, without having to design and fabricate a complete converter.

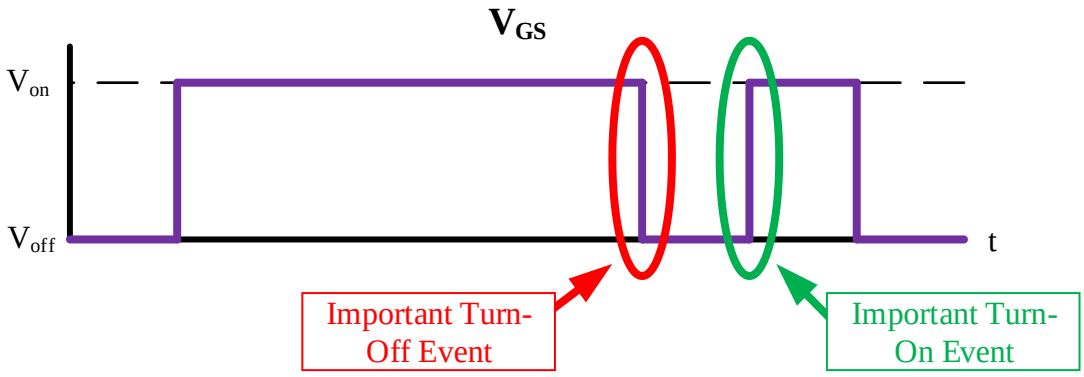
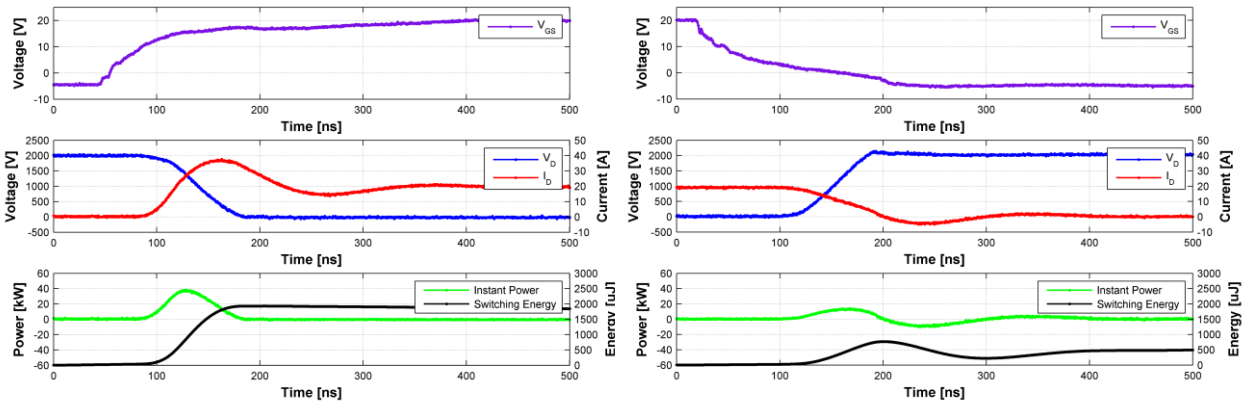


Figure 18: Identification of important DPT switch events

To obtain an estimate of switching losses from a DPT, the DUT's instantaneous current and voltage waveforms are multiplied to obtain the instantaneous power at each point during the switch transition. The instantaneous power is then integrated across each switching event to estimate the energy dissipated during that event. This process, shown in Figure 7, is performed for the turn-off and turn-on waveforms, and the resulting energy estimates are summed to determine the total switching loss of the DUT. Figure 19 shows an example of these calculations during (a) turn-on and (b) turn-off events for a DUT operating at 2 kV and 20 A [54]. The top two subplots show direct measurements from the DPT, while the bottom subplot shows calculated power (green) and energy (black) associated with these switching events. This

analysis produces a single switching energy value for the DUT at the tested operating condition. To estimate the average switching power loss in an application such as a dc-to-dc converter, this energy is then multiplied by the switching frequency of the semiconductor as shown in Equation (6).



(a) (b)

Figure 19: Example switching loss waveforms during (a) turn-on and (b) turn-off [54]

4.2. DPT Advantages

As stated earlier, one of the advantages of the DPT is the ease of controlling the operating conditions of the DUT, but another benefit revolves around the device thermals. Since this technique only requires two pulses and the entire test generally lasts less than 500 µs, the DUT and other components in the circuit do not have time to significantly heat up. Thus, the thermal stress applied to the circuit, and most importantly, the DUT, is minimal. This allows the DUT to be evaluated at its peak power ratings without a thermal management solution.

A more subtle advantage of DPTs is the ability to separate the losses due to turn-on and turn-off. Using CCO, only the total loss over one switching period can be extracted, but in DPT, the losses due to turn-on and turn-off can be individually estimated. This additional tool allows application designers to tune a converter to optimize each loss mechanism separately.

A final advantage of the DPT is the open-loop nature of the test. When using loss techniques that require a converter to operate at full load, generally this is integrated with closed-loop control which requires increased design effort. The DPT does not require feedback or a controller to operate effectively.

4.3. DPT Metrology Consideration

The main challenge with the DPT procedure is satisfying the metrology requirements necessary to accurately measure the device's characteristics. The instrumentation must be able to measure high-frequency content expressed on high-amplitude signals with good fidelity while having minimal impact on the circuit being measured. This section outlines these challenges in more detail.

4.3.1. Bandwidth

The first and often most difficult challenge with DPT metrology is providing sufficient bandwidth (BW) to capture the high-frequency dynamics present in the DUT switching waveforms. These high-frequency dynamics are split into two categories: first, the underdamped oscillations that appear on the voltage and current waveforms after switch transitions; and second, the equivalent frequency associated with the DUT switching edges. The requirement imposed by the first category, underdamped oscillations, can be realized by evaluating the literature. SiC-based circuits are regularly observed with significant oscillatory content up to 70 MHz [36], [55]. The second category, the equivalent frequency of the DUT switching edges, can be quantified by calculating the effective bandwidth of a linear ramp signal using Equation (9) [52].

$$f_{eff} = \frac{0.35}{\min(t_r, t_f)} \tag{9}$$

where t_r is the signal's rise time in nanoseconds, t_f is the signal's fall time in nanoseconds, and f_{eff} is the signal's effective bandwidth in GHz. The metrology must therefore be capable of accurately measuring the highest frequency component present in these two categories which is summarized in Equation (10).

$$f_{max} = \max(f_{osc}, f_{eff}) \tag{10}$$

where f_{osc} is the highest frequency present in the underdamped oscillations after the switch event, f_{eff} is the signal's effective bandwidth during switching transitions, and f_{max} is the maximum frequency present in the signals of interest.

According to the Nyquist-Shannon sampling theorem, a signal must be sampled at twice the maximum frequency present to perfectly recreate the signal [56]. Most modern oscilloscopes have bandwidths in the hundreds of megahertz to gigahertz range which is sufficient to satisfy the 2x sampling requirement. Often the limitation in practical systems is therefore the bandwidth of the oscilloscope and oscilloscope probes. The actual measurement bandwidth is the combination of the cascaded bandwidth from the oscilloscope and probe which is calculated using Equation (11) [57].

$$BW_{sys} = \frac{1}{\sqrt{\frac{1}{BW_{osc}^2} + \frac{1}{BW_{probe}^2}}} \tag{11}$$

where BW_{osc} is the bandwidth of the oscilloscope, BW_{probe} is the bandwidth of the oscilloscope probe, and BW_{sys} is the system bandwidth which is the cascaded bandwidth of the probe and oscilloscope together.

The rated bandwidth of each component is typically provided at the 3 dB point of the component's frequency response. This implies that at the rated bandwidth, the measured signal

magnitude is approximately 70% of the actual signal magnitude [57]. For this reason, it is necessary to increase the bandwidth margin beyond simply having bandwidth equal to the signal frequency. The suggested rule of thumb is a factor of 5x over the maximum frequency for adequate magnitude fidelity and 10x over the maximum frequency for adequate phase fidelity [57]. The influence of metrology bandwidth is illustrated in Figure 20, which shows a fast-rising voltage signal transition with an effective frequency of 70 MHz computed from Equation (9). The waveforms in this figure represent simulated measurements using voltage probes with different bandwidths. Analysis of the figure shows that when the probe BW is equal to the equivalent frequency of the signal of interest (BW = 1x), the measurement does not accurately represent the original signal with high fidelity. The simulated measurement does not have good agreement with the reference signal until the probe BW approaches ten times the effective frequency of the signal of interest. This agrees with the rules of thumb discussed in [57]. In the example 70 MHz case, this implies that the BW of both the oscilloscope and the probe must be greater than 700 MHz to provide high-fidelity measurements. Measurement equipment with these bandwidths at the power levels required to characterize WBG devices are often cost prohibitive or difficult to integrate into a practical characterization platform.

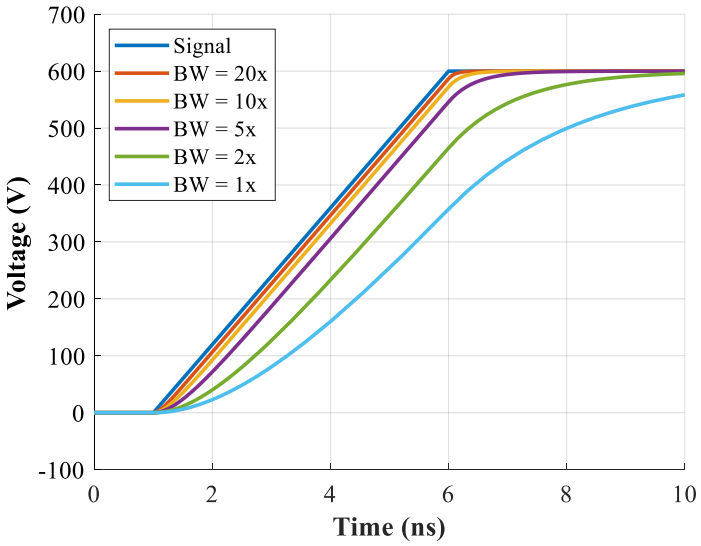


Figure 20: Simulation demonstrating influence of voltage probe BW on a fast-rising signal

4.3.2. Influence of Metrology on the Circuit

At the frequencies present in WBG measurements, the impact of the instrumentation on the circuit cannot be ignored. For example, passive oscilloscope voltage probes have input capacitance that may load the circuit being evaluated. To ensure accuracy in DPT results, all probes must have minimal parasitics. Otherwise, the impedance loading of the probes can substantially influence the measurement results, as well as the actual behavior of the circuit and DUT.

The connections of probes to the oscilloscope can also create undesired circuit loops that allow currents to flow though the oscilloscope instead of the circuit. The shields of probe attachment points on most oscilloscopes are internally connected together and to the oscilloscope's chassis ground, which is usually attached to building (earth) ground. This connection between the shields provides more accurate measurements since the signals are all referenced to the same plane, and the connection is grounded for safety considerations. One undesired consequence of these interconnections is that the probe shields, which connect to the test circuitry in different locations, can be subjected to different voltage potentials by the circuit.

If the shields of these probes are spaced physically apart, currents flow through the loop created by the probe shields, which can substantially influence the measurement results. When performing DPTs using probes without galvanic isolation, it is necessary to attach all the probe shields in a tight pattern to reduce the likelihood of voltage potential differences between the shields.

Alternatively, the ground loops created by probe attachment points can be mitigated by employing probes that provide galvanic isolation between the circuit and the oscilloscope. For current measurements, Hall Effect sensors, Rogowski coils, or current transformers (CTs) provide galvanic isolation. Unfortunately, these techniques have limited bandwidth compared to alternative methods that do not provide galvanic isolation, such as a current shunt [55]. The bandwidth of Hall Effect sensors and Rogowski coils are generally too low for use in WBG applications (less than 10 MHz). High-performance CTs are available with bandwidth in the 200 MHz range. However, these sensors have a small measurement aperture that makes it very difficult to integrate into a well-designed circuit without negatively impacting the circuit performance [55]. In fact, the added parasitics involved with routing circuit conductors through the small CT aperture may dominate the parasitics of the circuit under analysis. For voltage measurements, differential voltage probes can be used to isolate the circuit under analysis from the oscilloscope. However, differential voltage probes have significantly lower bandwidth and dynamic range compared to passive voltage probes, which is typically not acceptable for WBG measurements [52].

4.3.3. Limits of Integration

Another challenge associated with DPT analysis is precisely determining the start and stop times of the individual switching events. Since switching energy is calculated by integrating

the instantaneous power during the switch event, changing the time bounds of the switching event can significantly affect the loss estimation. Several authors have provided guidelines on how to select the integration bounds to achieve the most accurate results, but these techniques cannot be universally applied across all waveforms and still require a human to make a subjective decision [52], [54], [58]. According to the author's knowledge, there is no set of rules that can be universally applied as an algorithm to all switching waveforms. Figure 21 provides a visual representation of the challenge with selecting integration bounds.

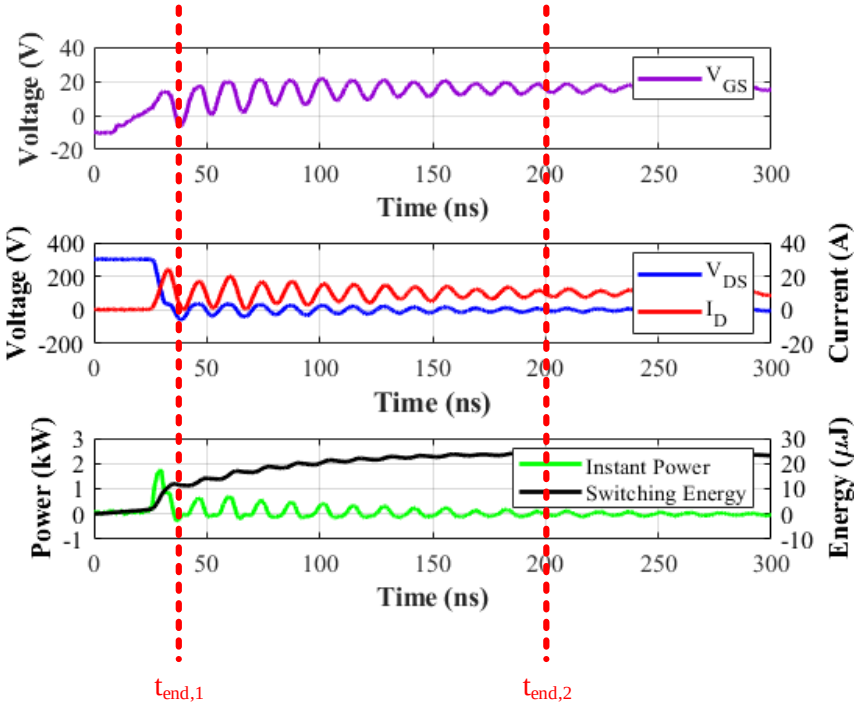


Figure 21: Representation of the challenges of selecting DPT integration bounds

The waveforms shown in Figure 21 are for the turn-on event of a cascade GaN HEMP from Transphorm operating at 300 V and 10 A [59]. If the end limit of the integration interval is selected to be the first negative sloped zero-crossing of the power waveform (indicated as $t_{end,1}$), the energy estimation is 12.0 µJ. If the end limit of integration is selected to be a negative sloped zero-crossing once most of the oscillation have stopped (indicated as $t_{end,2}$), then the energy

estimation is 23.9 µJ. This simple difference in the end limit of integration can result in a dramatic difference in estimated loss.

Although these bound restrictions are presented here as a major challenge, this issue is generally only pronounced when using aggressive edge rates or in the presence of poor metrology such as measurement offsets. The waveforms presented in Figure 21 were generated using a low gate resistance value typically not used in applications to exacerbate the limits of integration issue. Generally, the difference in energy values due to different limits of integration bounds are significantly smaller, assuming at least one or more of the guidelines described in the literature are observed when selecting the bounds. The author recognizes this issue will become more pronounced in the future as nominal edge rate continue to increase and work is being done to make the selection of integration bounds less subjective for future analysis. In this work, more reasonable gate resistance values were selected to indicate more clear limits of integration bounds.

4.3.4. Time-Alignment between Signals

DPT relies heavily on the time-alignment between the current and voltage measurements in order to produce accurate estimates of switching loss. Since the loss estimation is derived from the integration of the instantaneous power, it is essential that the power calculation involves current and voltage measurements that are precisely aligned. With the fast edge rates commonplace with WBG technology, the entire switching event can happen in only tens of nanoseconds, so even the propagation delays in the probe leads cannot be ignored. Figure 22 shows an example from DPT data of the impact that timing misalignment can have on switching energy estimates. As the misalignment deviates from the perfect alignment (0 ns), a linear error term is introduced into the estimates of turn-on and turn-off loss. As shown in Figure 22, the vast

majority of this error involves the “relocation” of energy from the turn-on to the turn-off transition and vise-versa. It has been shown that some measure of timing misalignment can be tolerated so long as the emphasis is on the total, per-cycle switching energy instead of separate turn-on and turn-off losses [30]. However, to achieve greatest accuracy and the ability to separate turn-on and turn-off losses, timing misalignment in the measurement setup must be eliminated through one of several methods presented in the literature [52].

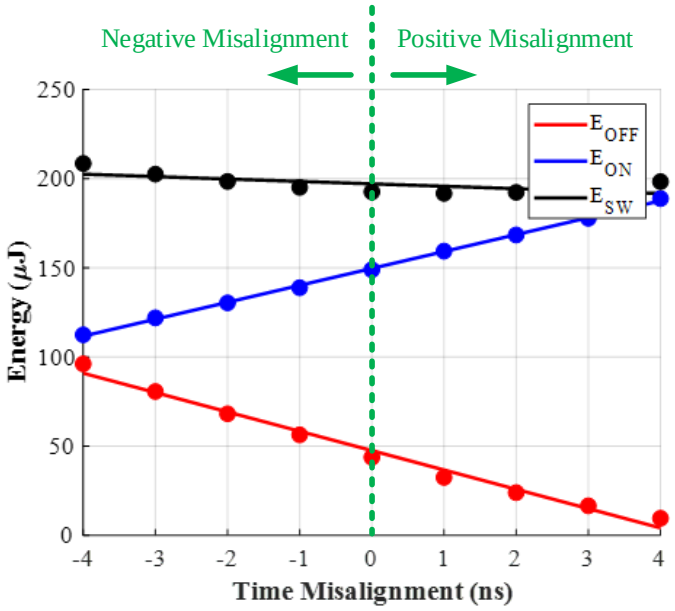


Figure 22: Effect of time misalignment on switching loss estimations

4.4. DPT Circuit Considerations

The second challenge with DPT analysis has to do with the circuit surrounding the DUT. When designing the DPT test fixture, poor printed circuit board (PCB) layout practices can create circuit parasitics that significantly influence DPT results. These fixture parasitics can lead to undesired circuit dynamics that are the result of the test fixture, not the DUT. In addition to the test fixture PCB layout, the ancillary circuit elements required for the DPT procedure can also impact loss estimations. This section outlines some of the requirements for the DPT circuit elements.

4.4.1. DC Link Capacitors

In practice, the input voltage shown in Figure 15 is generally a large capacitor bank or a power supply unit in parallel with a large capacitor bank. The first requirement for these capacitors is that they must have sufficient energy storage to support the DPT sequence without permitting substantial droop in the input voltage rail. Second, the capacitors need to be placed physically close to the DUT since all the DUT current must also flow through this capacitor bank. Third, the capacitors must have low parasitic inductance to prevent introducing additional oscillations in DPT measurements, as the equivalent series inductance (ESL) of these capacitors appears in series with the inductance of the dc bus in the DPT circuit.

4.4.2. Freewheeling Diode

Traditional PN-junction diodes suffer from reverse recovery losses which occur when a diode transitions from conducting current (forward biased) to blocking voltage (reverse biased). In a PN-junction diode, the forward current flow is supported by the movement of both electrons and holes which results in electrons building up in the p-region of the diode and holes in the n-region [5]. When the diode stops conducting, this configuration allows a negative current flow through the diode for a short period of time, which is called reverse recovery. While the diode is conducting reverse current, it becomes reversed biased and starts to block voltage. This results in power loss because the diode is simultaneously conducting current and blocking voltage [5]. Therefore, for DPT analysis, it is recommended to use Schottky diodes for the freewheeling element to eliminate the reverse recovery losses; Schottky diodes still incur capacitive recovery losses, but these losses are significantly smaller than reverse recovery losses.

4.4.3. Load Inductor

One major requirement when selecting or designing the load inductor for a DPT setup is its self-resonant frequency (SRF). The SRF must be high enough such that is not excited by the switching transitions of the DUT to avoid introducing additional oscillations into the DPT waveforms. Inductors with many winding layers routed in close proximity to one another should be avoided due to the large inter-winding capacitance that is created between the layers. A guide to designing high-performance inductors with high SRF values is provided in [60].

When the DPT sequence was first introduced in this thesis, it was assumed that the inductor would have a linear current ramp with respect to time under a constant voltage stimulus. This assumption is only true when the inductor operates in the linear region of the core material's BH curve. If the load inductor core is selected incorrectly, the inductor current waveform will have non-linear behavior due to saturation of the inductor core. Depending on the selection of core material, this saturation may be gradual (usually the case with distributed air-gap cores) or it may be abrupt (usually the case with ferrite cores). Figure 23 demonstrates the effect of gradual saturation of the inductor core on the measured load inductor current during a DPT sequence.

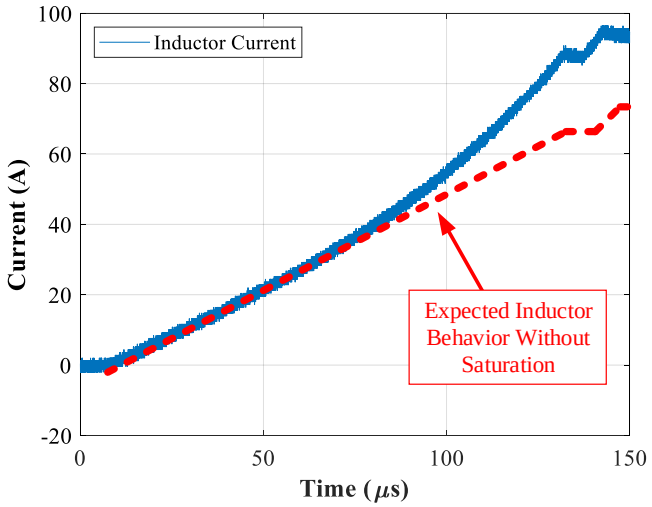


Figure 23: Effect of saturation on DPT inductor current

Any non-linear behavior contributed by the load inductor core causes challenges during DPT operation. First, the non-linear behavior makes it difficult to precisely control the operating current of the DUT. Second, and more importantly, inductor saturation risks damaging the DUT or other components in the circuit since the current device may increase very quickly, depending on the type of core material employed.

4.4.4. Shoot-Through

A final challenge associated with the DPT process is the possibility of a phenomenon called shoot-through. Often, DPT is used to evaluate multi-chip power modules (MCPMs) in the half-bridge configuration instead of discrete semiconductor devices. A simplified schematic for this configuration is shown in Figure 24. In a half-bridge DPT, one of the switch positions of the half-bridge remains off for the entire DPT. This allows the "inactive" switch to be used for the freewheeling diode (either the MOSFET body diode or an anti-parallel diode in the module can serve this purpose). However, under certain circumstances, the inactive switch can turn partially or fully on, which results in a significant increase in DUT current. This phenomenon is called shoot-through, since turning on both switch positions in the half-bridge configuration effectively attaches a low-impedance connection across the dc supply.

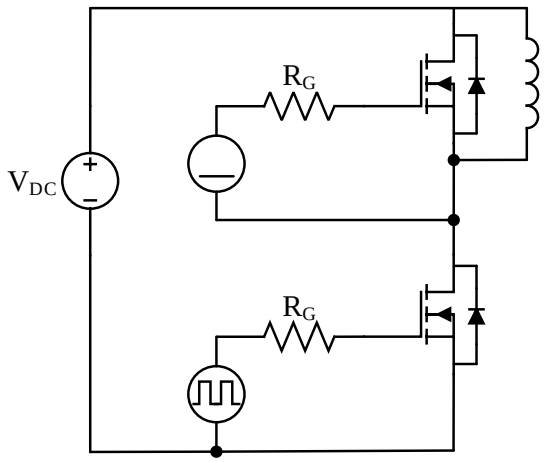


Figure 24: DPT configuration for half-bridge MCPM

Even if the inactive switch does not turn fully on during the DPT sequence, its presence in the circuit still influences the switching loss of the half-bridge configuration. In fact, it has been shown in the literature that the losses from both the active and inactive switches must be considered to accurately estimate switching losses of the half-bridge topology [52]. The high dv/dt caused by the operation of the active switch can create spurious voltage pulses on the gate of the inactive switch. These spurious voltage pulses can cause the inactive switch to turn on, resulting in shoot-through. When this occurs, the switching loss of the inactive switch can reach levels similar to the switching loss of the active switch. DPT switching loss inaccuracy caused by shoot-through can be mitigated by adding a second current measurement for the inactive switch or by using alternative techniques as proposed in [52].

4.5. DPT Summary

Double-pulse testing can be used to estimate the switching loss for active semiconductor devices without the need for a thermal management solution. This approach also supports precise control of the DUT's operating conditions, which provides significant flexibility during device characterization. However, there are some challenges associated with the application of this technique. Specifically, care must be taken to ensure that the metrology requirements are adequately addressed, and that the influence of the test fixture on the resulting measurements is minimized. However, when the guidelines described in the literature are followed, the DPT technique is a powerful and flexible tool for estimating switching loss.

CHAPTER 5:

EMPIRICAL TEST SETUP

A valid comparison between the loss estimation methods requires evaluating both techniques described previously, CCO and DPT, with similar bus work geometry and metrology. This section describes the hardware used to evaluate the two techniques.

5.1. Bulk Capacitor Printed Circuit Board

This work leveraged a platform that has been described in previous publications for characterizing devices using DPTs [61]-[62]. Figure 26 shows the Bulk Capacitor PCB and includes labels for several of its components. The two main purposes of this platform are to provide operators with a safe and consistent method to perform tests; and to serve as a base to limit the amount of work necessary to evaluate several devices ranging in size and ratings. Often, a significant portion of a test setup's cost is for the bulk capacitors which are needed to maintain a steady input voltage for the duration of the test. In setups that are customized for each device being evaluated, the cost of the capacitors must be included in each design. However by using this platform, the same bulk capacitors can be used across a range of tests. The PCB for this platform is designed such that a second PCB, referred to as an adapter board, is attached to the right side of the board and utilizes the bulk capacitance found on this PCB.

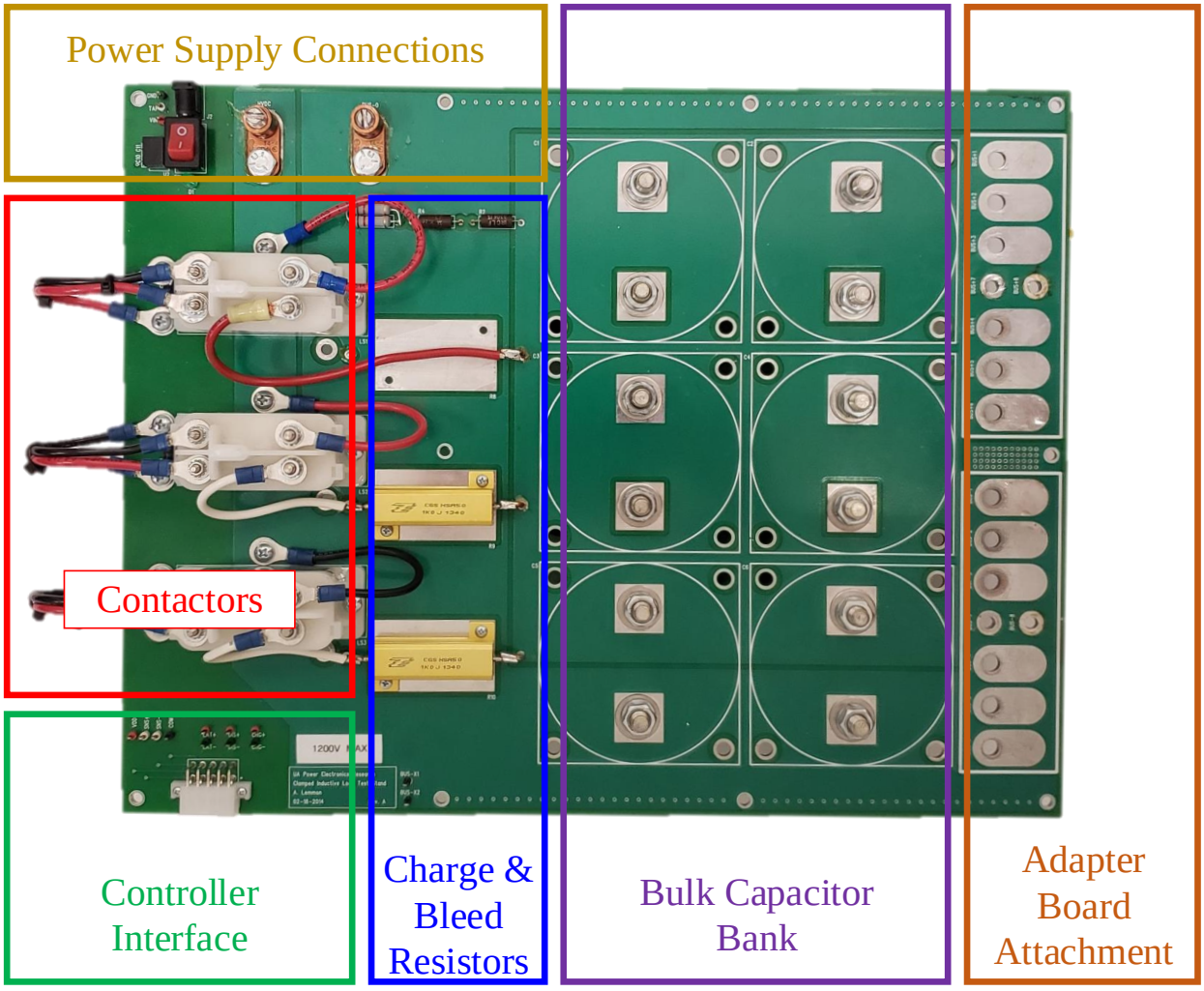


Figure 25: Bulk Capacitor PCB

Since the bulk capacitors on this board will be used across a range of tests, it is important that they have sufficient energy storage to perform high-power tests with minimal inductance between the connections. This platform uses six capacitors attached in parallel to form a large capacitance. Each capacitor is made of polypropylene with a rating of 220 µF and 40 nH [63]. The parallel combination of these capacitors results in a total capacitance of 1320 µF and less than 7 nH of inductance. This total capacitance is referred to as C_{BULK}. Before performing a DPT, the capacitors are charged using a power supply unit to the desired operating voltage, but before the test is performed, the PSU is disconnected from the platform using contactors. This

separation occurs for two reasons: (1) to prevent damage to the PSU in the case of a catastrophic failure of the DUT, and (2) to remove additional parasitic paths for current flow through the test equipment. The capacitors have current limiting resistors (R_{CHARGE}) in series with the PSU to prevent surge charging. After testing is complete, a contactor is used to connect the bus to a small resistance ($R_{DISCHARGE}$) which quickly discharges the bus. In addition, a large resistor (R_{BLEED}) is always connected across the capacitors. The bleed resistance value is high enough such that it does not affect the DPT results, but it ensures that the capacitors are not accidentally left at dangerous voltage potentials after testing is completed. The circuit is controlled by a handheld device which allows an operator to charge and discharge the capacitor bus voltage using momentary buttons from a safe distance. The schematic showing the electric components of the Bulk Capacitor PCB is shown in Figure 26.

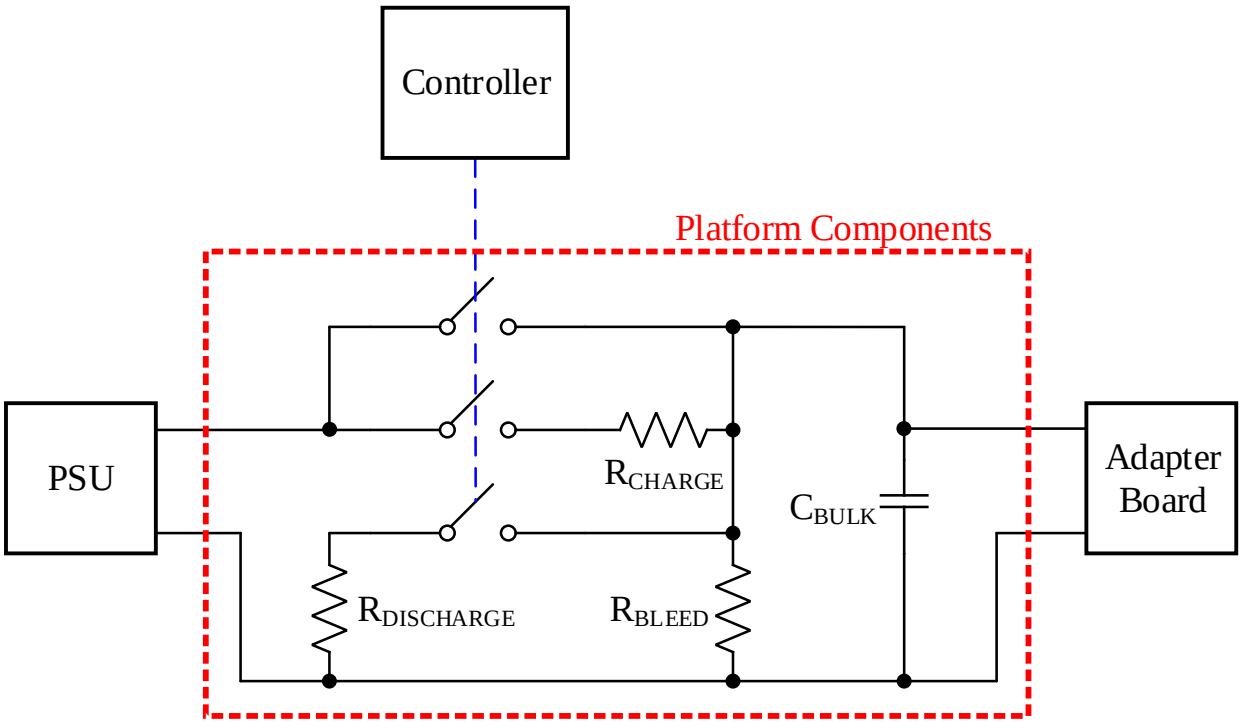


Figure 26: Schematic of the Bulk Capacitor PCB

5.2. Adapting the Bulk Capacitor PCB for CCO

Although the bulk capacitor PCB was designed for DPTs, the modularity of the board allows it to operate seamlessly as the input capacitance of a converter with few modifications to the platform. Bypassing the charge resistor and operating the setup with the charging contactor always on allows the platform to operate continuously. In this manner, both the DPT and CCO configurations can be operated from the same PCB. For both switching loss configurations, this platform only serves as the input capacitance for the actual circuit measurements, so an adapter board was utilized for adding the remaining circuit elements.

5.3. Converter Type Considerations

Since one of the main disadvantages of the CCO technique is the difficulty in isolating the losses due to the DUT, it was desired to use a converter topology with minimal complexity when performing the CCO evaluation to reduce the other potential losses in the system. For this reason, the buck and boost converter topologies were considered for the CCO measurements. These two circuits, without showing parasitic elements, are shown in Figure 27 where q is the control signal for the DUT. In this section, these two topologies will be introduced and evaluated based on the advantages and disadvantages with regards to this work.

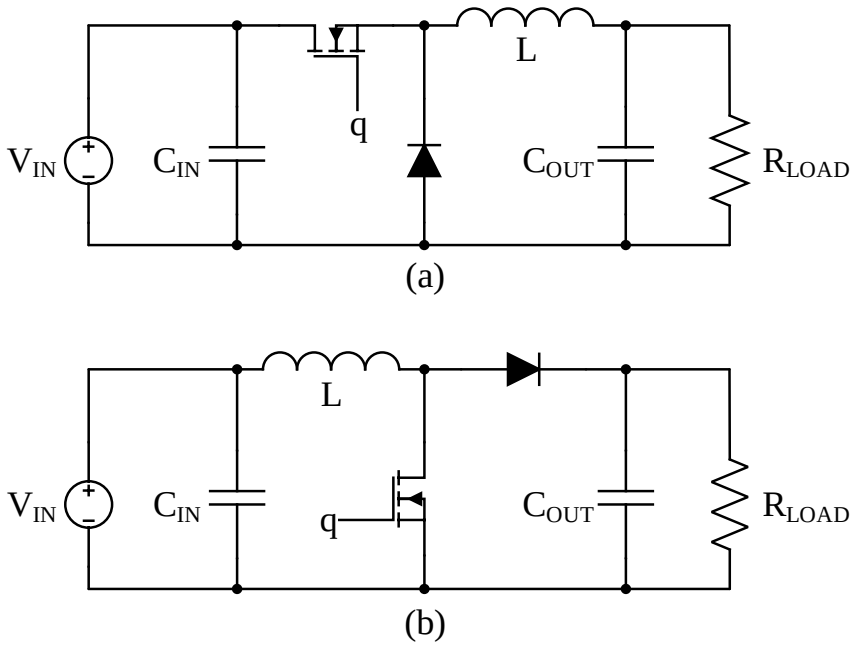


Figure 27: Schematic of (a) buck converter and (b) boost converter

5.3.1. Buck Converter

In a buck converter, a voltage is stepped down from a higher voltage to a lower voltage following the relationship shown in Equation (1) [5].

$$\overline{V_{OUT}} = D\overline{V_{IN}} \tag{12}$$

where $\overline{V_{IN}}$ is the converter's average input voltage, $\overline{V_{OUT}}$ is the converter's average output voltage, and D is the duty cycle of the DUT. It should be noted that due to the losses in the system and the non-instantaneous turn-on and turn-off transitions, this relationship will deviate slightly from Equation (1). If the converter was 100% efficient, then the input power would equal the output as shown in Equation (13) or equivalently in Equation (14).

$$\overline{P_{IN}} = \overline{P_{OUT}} \tag{13}$$

$$\overline{V_{IN}} \cdot \overline{I_{IN}} = \overline{V_{OUT}} \cdot \overline{I_{OUT}} \tag{14}$$

where $\overline{P_{IN}}$ is the converter's average input power, $\overline{P_{OUT}}$ is the converter's average output power, $\overline{I_{IN}}$ is the converter's average input current, and $\overline{I_{OUT}}$ is the converter's average output current.

Since the voltage follows the relationship shown in Equation (12), this suggests that the current follows an inverse relationship with duty cycle as described in Equation (15). Once again, this is an idealized expression.

$$\overline{I_{OUT}} = \frac{1}{D}\overline{I_{IN}} \tag{15}$$

A buck converter operates by splitting the switching period into two states: (1) conducting current from the input voltage to the load, and (2) freewheeling current through the diode. While the semiconductor is in the on-state, there is a connection between the input power and the load that allows current to flow. In this state, the diode is reversed biased and energy is stored in both the inductor and the output capacitor and supplied to the load. This state is shown in Figure 28(a). While the semiconductor is in the off-state, there is no longer a connection between the input and output of the converter. Instead, the charged inductor completes a loop with the diode and the current "freewheels" through the diode. This state is shown in Figure 28(b).

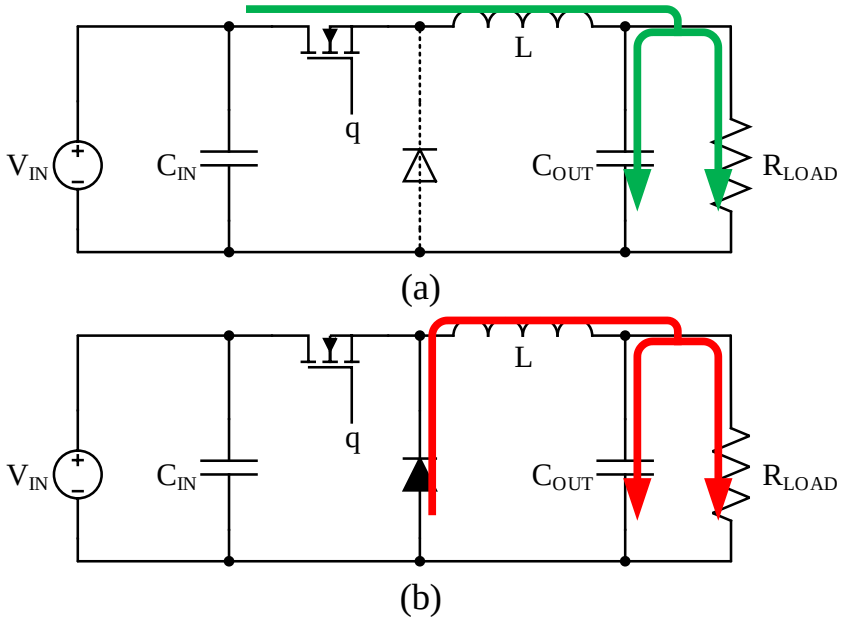


Figure 28: Buck converter (a) on-state and (b) off-state

The advantage for using a buck converter in the CCO evaluation is the ease of controlling the operating conditions for the device under test. When the device is off, it has no current flowing through it, and when it is on, it conducts the current going through the load; so the device switches between 0 A and I_{OUT}. For voltage, when the device is on, it does not block any voltage, and when the device is off, it blocks the entire input voltage, V_{IN}. Therefore, the operating conditions of the DUT are the input voltage and the output current. To compare DPT results to CCO results, it is essential that the evaluation is being performed at the same operating conditions, so the operator needs to ensure the converter is operating with the DUT at the proper operating conditions. For a buck converter, the operator only needs to set the input voltage to the desired level and then tune the duty cycle to get the desired output current.

The main challenge with using the buck converter setup revolves around the metrology. This work seeks to use the same circuit for the DPT and CCO with as few modifications as possible. As stated previously, DPTs are typically performed on the low-side of a half-bridge so that ground referenced probes can be used. In the buck converter, the source terminal of the MOSFET is connected to the switching node, not the negative rail of the input voltage. Therefore, in this configuration, only differential probes can be used to measure the drain-to-source and gate-to-source voltages. This introduces additional measurement error due to challenges associated with the amplifier within the differential probe.

5.3.2. Boost Converter

In this topology, the input voltage is stepped up to a higher voltage following the relationship shown in Equation (16) [5]. Similar to the buck converter, the relationship between the input current and output current in a boost converter is the inverse duty cycle ratio as shown in Equation (17).

$$\overline{V_{OUT}} = \frac{1}{1-D}\overline{V_{IN}} \tag{16}$$

$$\overline{I_{OUT}} = (1-D)\overline{I_{IN}} \tag{17}$$

The boost converter also has two main operating states. When the DUT is in the on-state, the series combination of the inductor and the on-state resistance of the device is the dominate impedance attached across the input voltage, so the inductor is charged. In this state, the output of the converter is essentially disconnected from the input voltage source and therefore, the output capacitor discharges through the load resistor. This state is shown in Figure 29(a). When the DUT is in the off-state, a loop is formed between the input supply and the output of the converter so some of the energy that was collected in the inductor during the charging process is passed along to the load. This state is shown in Figure 29(b).

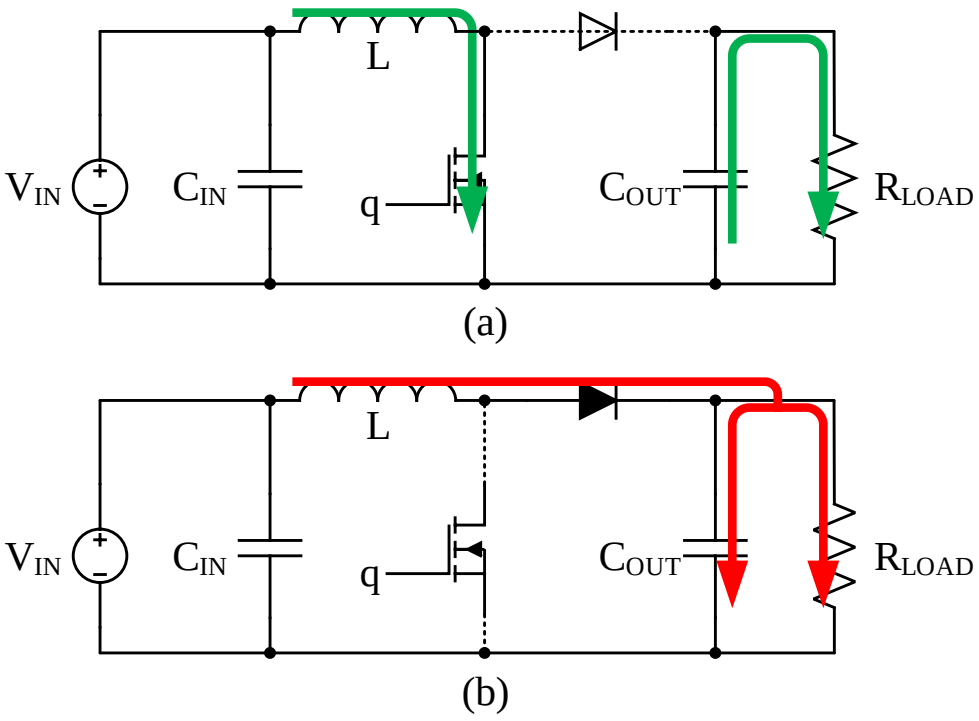


Figure 29: Boost converter (a) on-state and (b) off-state

While the converter is in the on-state, the DUT conducts the entirety of the input current and while off, conducts no current. For voltage, while in the off-state, the DUT blocks the output voltage, and while on, does not block any voltage. Therefore, contrary to the buck converter, the DUT in the boost converter blocks the output voltage (V_{OUT}) and conducts the input current (I_{IN}).

The voltage blocked and current conducted by the DUT in a boost converter pose a problem when tuning the converter for specific operating conditions. This is the main disadvantage of using a boost converter for the CCO evaluation. Controlling these two operating conditions is more challenging that the parameters in a buck converter because two variables (input voltage and duty cycle) must be tuned rather than just one (duty cycle) for a buck converter. The reason for the additional variable tuning is best understood through an example. Assume an operator is targeting a situation where a DUT switches 20 A and 600 V. At start-up, the converter reads an input current of 20 A as desired, but the output voltage is less than the target voltage. The operator, understanding the relationship between voltage and duty cycle, increases the duty cycle to increase the output voltage. The output voltage increases as expected, but since the load resistor remains constant, the output current therefore increases along with the input current. At this stage in the example, the input current exceeds the desired operating condition. In this situation, although the output voltage may be correct, the input current is higher than the intended operating conditions. This illustrative example is shown visually in Figure 30. To counteract the issues associated with only modifying duty cycle, the input voltage must be tuned in tandem with the duty cycle to achieve the intended operating conditions.

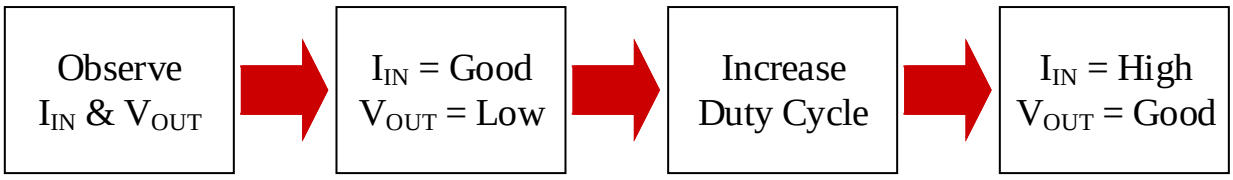


Figure 30: Example of challenges tuning DUT conditions in boost CCO

The main advantage of the boost converter is the significant improvements in the metrology compared to the buck converter. In this configuration, the DUT's source terminal is referenced to the PSU return line which means the setup can utilize ground referenced voltage oscilloscope probes instead of differential probes when using the board as a DPT. This provides the operator with DPT measurements that are significantly more accurate [52].

5.3.3. Converter Selection

The operating parameters of the DUT in the two converter types are summarized in Table 1. The reason for the emphasis on understanding the DUT properties is that for this comparison, it is essential that the DUT blocks the same voltage and conducts the same current in both the DPT and CCO analysis to ensure the switching losses can be compared.

TABLE 1: DUT OPERATING CONDITIONS DURING BUCK AND BOOST CCO

	Current	Voltage
Buck	I_{OUT}	V_{IN}
Boost	I_{IN}	V_{OUT}

For this work, the boost converter was selected due to the increased accuracy in the DPT results. The primary downside of the boost converter is that it increases with the amount of time necessary to perform the experiments. The increased result accuracy was prioritized over the duration of tests.

5.4. Adapter Board

By utilizing the Bulk Capacitor PCB, some of the challenges with creating this comparison setup were already overcome. Still, it was necessary to design an adapter board which mounts to the Bulk Capacitor PCB. This circuit needs to easily operate as a converter and be used in DPT with minimal changes. In addition, the circuit must have the necessary

attachment points for the metrology used in both configurations (CCO and DPT). The necessary changes between the two circuit configurations is shown in Figure 31.

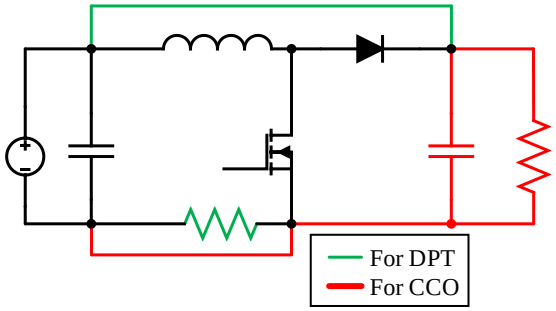


Figure 31: Differences in circuit design for DPT and CCO

For this work, a custom PCB was designed to be used as a boost converter and in DPT. The adapter board is shown in Figure 32 and the adapter board's attachment to the DPT platform is shown in Figure 33. Note that for both evaluations, the DUT was mounted to the underside of the board and attached to a cold plate to maintain the case temperature at a constant 18°C across all experiments. This section will describe several of the components used on the adapter board.

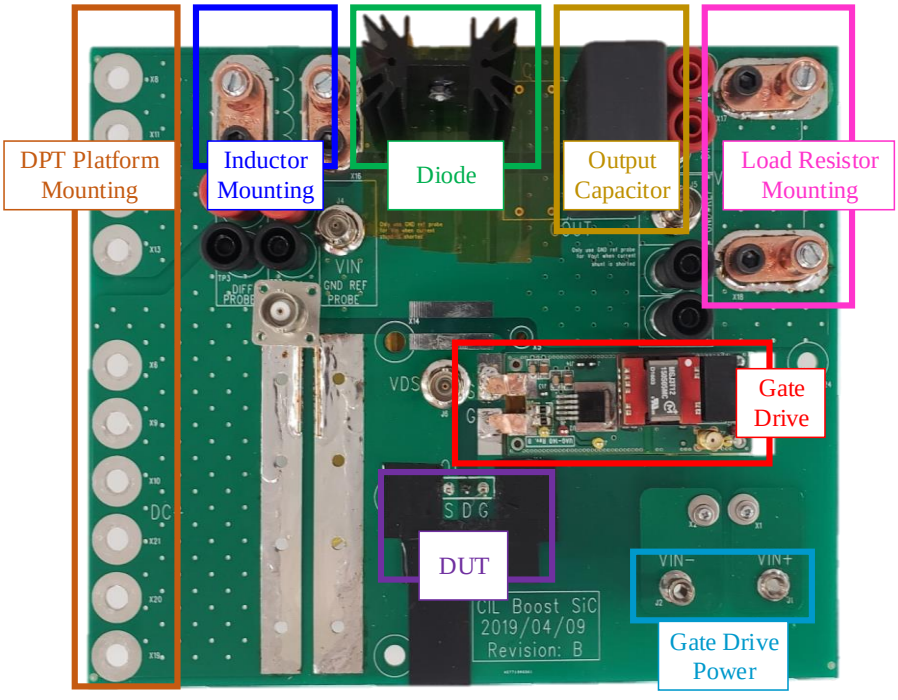


Figure 32: Adapter board circuit

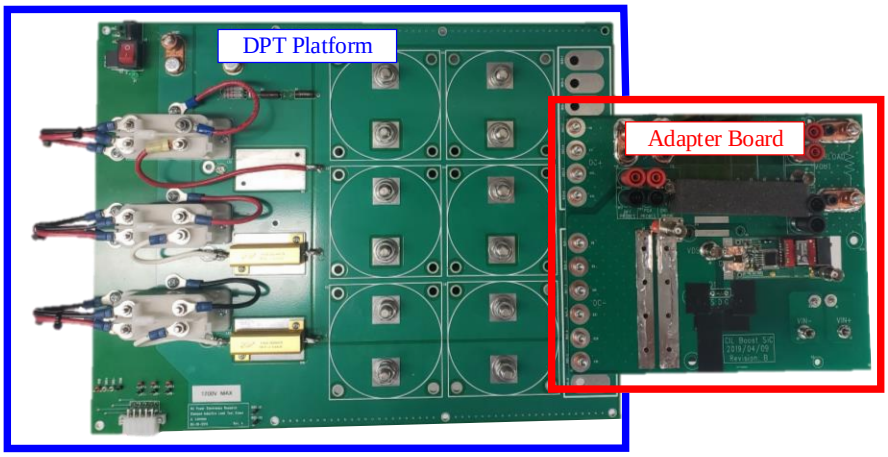


Figure 33: Adapter board attachment to the DPT platform

5.4.1. Device Under Test

The component used as the device under test in this evaluation was the LSIC1MO120E0080 silicon carbide TO-247 discrete MOSFET manufactured by Littelfuse [64]. The part is rated for 1200 V and 25 A (continuously), and has a nominal on-state resistance of 80 mΩ. As stated earlier, the DUT was mounted to a cold plate with liquid cooling maintaining the DUT's case temperature at 18°C for all the experiments described in this work.

5.4.2. Diode

The diode utilized in this setup was the C4D20120A silicon carbide Schottky diode manufactured by Cree [65]. The component is rated for conducting 20 A (continuously) and blocking 1200 V. The diode was fitted with a heat sink and forced air cooling was utilized for the duration of the testing. A Schottky diode was selected to eliminate reverse recovery losses.

5.4.3. Gate Driver

The gate driver is a custom design which features 3 kV of isolation on the signal pin and 5.2 kV of isolation on the power rails [66]-[67]. The output stage is driven by a totem pole MOSFET capable of driving 14 A and the setup uses a 5 Ω gate resistor [68]. This gate

resistance was selected because it is a value that would typically be used with this type of device in an application. Figure 34 shows the gate driver design.

Figure 34: Gate driver

5.4.4. Load Inductor

As stated previously, it is important that the self-resonant frequency of the inductor used in a DPT is not excited by the switching transitions of the DUT. Using the technique described in [60], an inductor bank was designed which has a total inductance of 623 µH, equivalent resistance of 220 mΩ, and SRF of greater than 20 MHz. The bank consists twelve series inductors each made with two stacked Kool Mµ cores with 17 turns a piece [69]. One of the individual inductors is shown in Figure 35(a) and the entire inductor bank is shown in Figure 35(b).

(a) (b)

Figure 35: Load inductor: (a) single inductor and (b) entire inductor bank

5.5. Metrology

This section explains the measurement equipment used in the two switching loss estimation techniques. Figure 36 shows the location of several of the probe attachment points

that will be discussed in this section. This figure does not show the input voltage and current measurement locations since these were attached to the input of the Bulk Capacitor PCB rather than the adapter board.

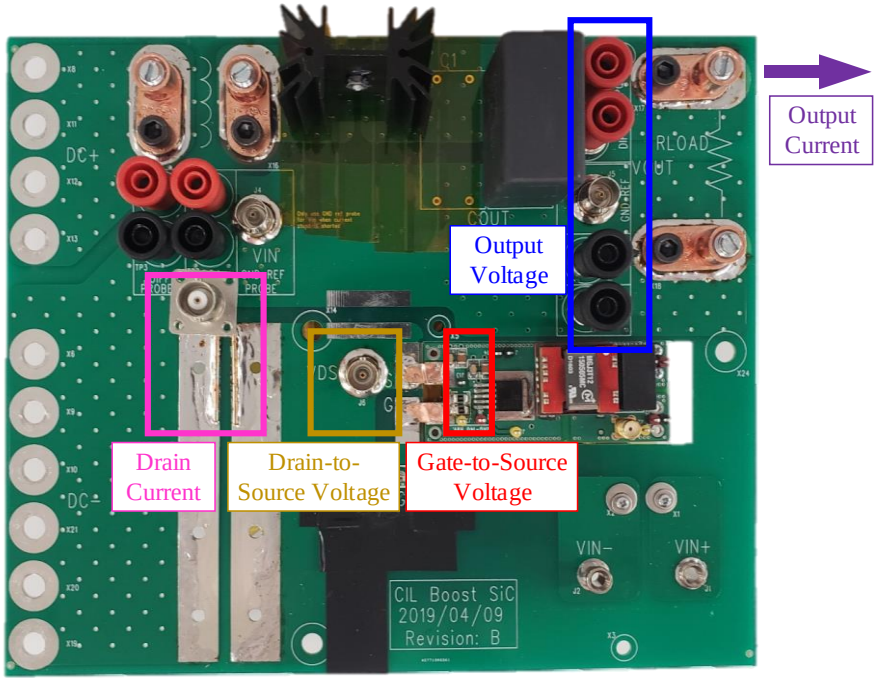


Figure 36: Adapter board metrology locations

5.5.1. CCO Metrology

For the CCO analysis, the only measurements that are needed are the converter's average input and output voltages and currents. These are used to calculate the input power, output power, and power loss of the converter. The locations of these four measurements are shown in Figure 37.

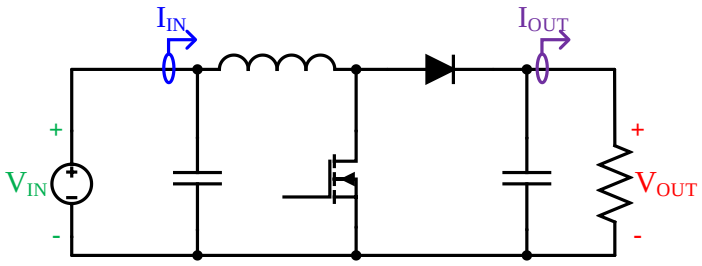


Figure 37: Metrology locations during CCO

Due to the known challenges with taking accurate, high-current measurements for extended durations, two measurement techniques were simultaneously used while in CCO. Using two techniques allows for a comparison with not only the DPT, but also the accuracies associated with the two separate CCO measurement techniques. The first method used a Tektronix PA4000 Power Quality Analyzer (PQA) shown in Figure 36 [50]. The PQA uses precision 30 A-RMS current shunts to measure the converter's current. It simultaneously samples the input and output currents and voltages. The instrument was configured to sample the converter every 0.2 s and log the data for the duration of the experiments. The power loss at each operating condition was determined by calculating the average power loss of the converter once it reached electrical and thermal steady-state.

Figure 38: PA4000 power quality analyzer

The second measurement used the Tektronix MSO58 oscilloscope shown in Figure 39. The probes used in the evaluation are summarized in Table 2. The oscilloscope was configured to sample the input and output voltages and currents at a rate of 62.5 MS/s. These measurements were averaged across one second of operation and used to determine the power loss at each operating condition. The one second oscilloscope averaging was repeated five times at each operating condition and the power loss across the five tests were themselves averaged to get a

single power loss estimation at each operating condition. This is the equivalent of averaging the power loss over five seconds, but has the advantage that it allows the oscilloscope to sample at a higher sampling rate than averaging the data over a single five second window.

Figure 39: MSO58 oscilloscope

TABLE 2: CCO OSCILLOSCOPE METROLOGY

	Metrology	Bandwidth	Limit
V_{IN}	Tektronix TPP0850	800 MHz	1 kV
I_{IN}	Tektronix TCP0030A	120 MHz	30 A
V_{OUT}	Tektronix TPP0850	800 MHz	1 kV
I_{OUT}	Tektronix TCP0030A	120 MHz	30 A

5.5.2. DPT Metrology

To perform the DPT with this adapter board, slight modifications had to be made to the circuit. The Tektronix TCP0030A current probes used in the CCO setup do not have sufficient bandwidth to capture the high-frequency dynamics of a DPT test. Therefore, to measure the drain current, a precision 100 mΩ coaxial current shunt was added to the source terminal of the MOSFET during the DPT operation [70]. This current shunt is seen in the box labeled “Drain Current” in Figure 36. The coaxial shunt was not added to the circuit during CCO because the shunt is not rated for continuous power. Alternative shunt sizes that could handle the power

levels were considered for this work, but these shunts did not a high enough signal-to-noise ratio for DPT measurements. During CCO operation, this location on the board is shorted with copper foil. For the DPT, the converter's resistive load and output capacitors are not necessary so these components were removed from the circuit. Finally, for the system to function properly as a DPT, the input bus was connected to the cathode of the diode. These changes are indicated in Figure 40.

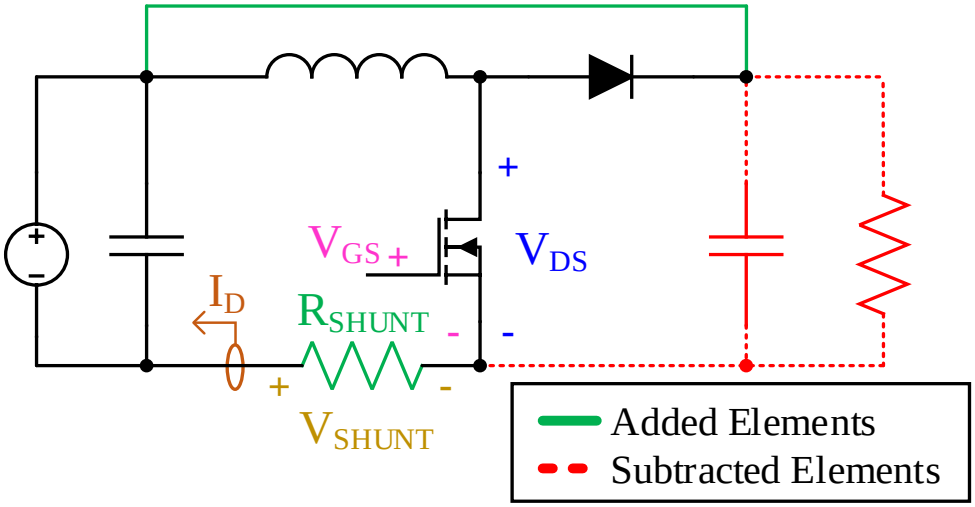


Figure 40: Metrology locations and circuit changes for DPT

As stated previously, the use of a boost converter for the CCO operation allows ground referenced probes to be used for the DPT. Table 3 shows the metrology used during the DPT characterization and the probe locations on the circuit are shown in Figure 40. The switching loss was estimated by integrating the instantaneous power in the DPT measurements over the duration of the switching events.

TABLE 3: DPT METROLOGY

	Metrology	Bandwidth	Limit
I_D	T & M Research SDN-10	2 GHz	2 J
V_{DS}	Tektronix TPP0850	800 MHz	1 kV
V_{GS}	Tektronix TPP0500	500 MHz	300 V

5.6. Test Operation

The steps required to actually perform the two types of tests differed slightly. This section explains how the two tests were performed.

5.6.1. CCO Testing

For CCO, the converter was switched continuously with switching frequencies from 100 kHz to 500 kHz at 100 kHz increments. A function generator was used to control the gate driver during these tests. At each switching frequency, the input voltage and duty cycle were tuned until the PQA was measuring an input current of 20 A and an output voltage of 600 V. Once these condition were met, the converter was operated continuously for at least ten minutes. The PQA logged the data at each switching frequency for the duration of the test. In post-processing, the power loss calculated by the PQA was averaged across the last five minutes of data at each switching frequency. This averaged data point was used as the power loss estimation for the PQA at each frequency. In addition to the PQA data, after the ten minutes of operation were reached, the power loss calculated by the oscilloscope was averaged across one second of operation. This one second averaging process was repeated five times, and these five power loss averages were once again averaged to reach a single loss estimation from the oscilloscope at each operating frequency.

5.6.2. DPT Testing

To ensure time alignment between the drain current and the drain-to-source voltage measurements, the setup was first deskewed using the third technique described in [52]. For this deskew process, the DPT inductor is replaced with a low-inductance resistor. The current through the DUT is estimated by considering the input voltage, voltage drop across the DUT,

and a precision measurement of the resistance. The deskew is completed by pulsing the DUT and time aligning the calculated current with the actual measured current.

Once the system was time-aligned, a microcontroller running custom firmware was used to generate a consistent charge pulse to get the inductor to 20 A at an input voltage of 600 V. Five DPTs were performed at these operating conditions, and the switching loss estimations from all five tests were averaged to get a single DPT loss estimation.

CHAPTER 6:

RESULTS AND ANALYSIS

The principle goal of this work is to compare the switching losses associated with two loss estimation techniques: DPT and CCO. In the preceding sections of this thesis, these two techniques were discussed in detail. These discussions included a description of expectations about their relative merits. However, empirical results are necessary to validate these claims. This section presents the results and analysis from the empirical testing that was conducted for this work.

6.1. Continuous Converter Operation Results

The boost converter discussed previously was configured with a 53 Ω load resistor and the switching frequency was operated from 100 kHz to 500 kHz at 100 kHz increments. Across all frequencies, the rated power of the converter was approximately 6.6 kW, and power loss calculations were performed with both a PQA and an oscilloscope. Figure 41 presents example input and output power measurements recorded with the PQA during twenty minutes of converter operation at a switching frequency of 100 kHz. The power loss was determined by computing the difference between the average value of the input and output power waveforms during each experiment. Figure 42 shows the power loss value computed at each considered frequency by both metrology configurations (PQA and oscilloscope).

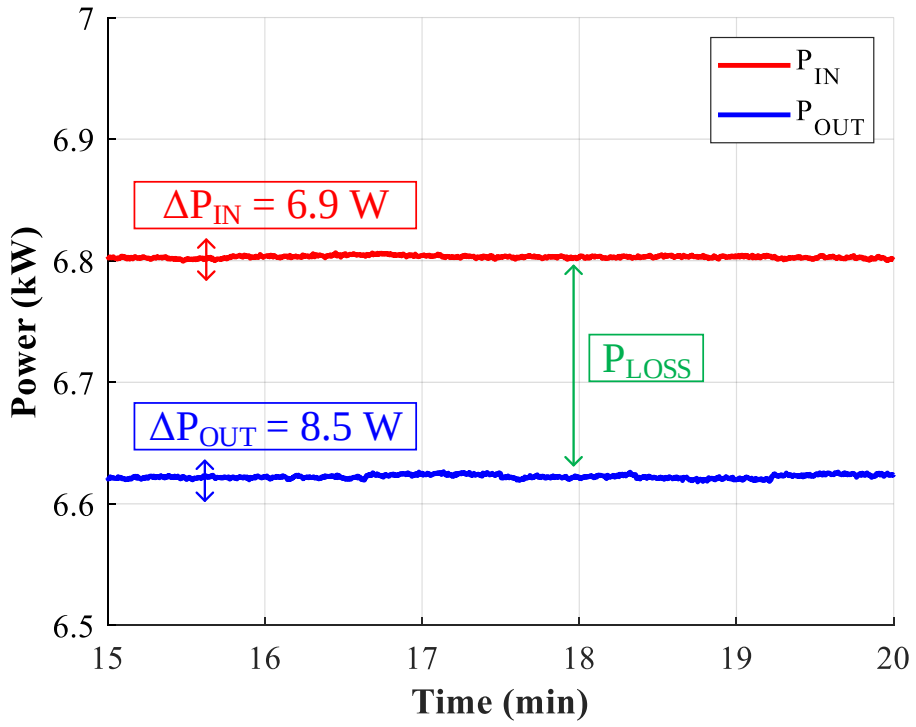


Figure 41: PQA input and output power during CCO at 100 kHz switching frequency

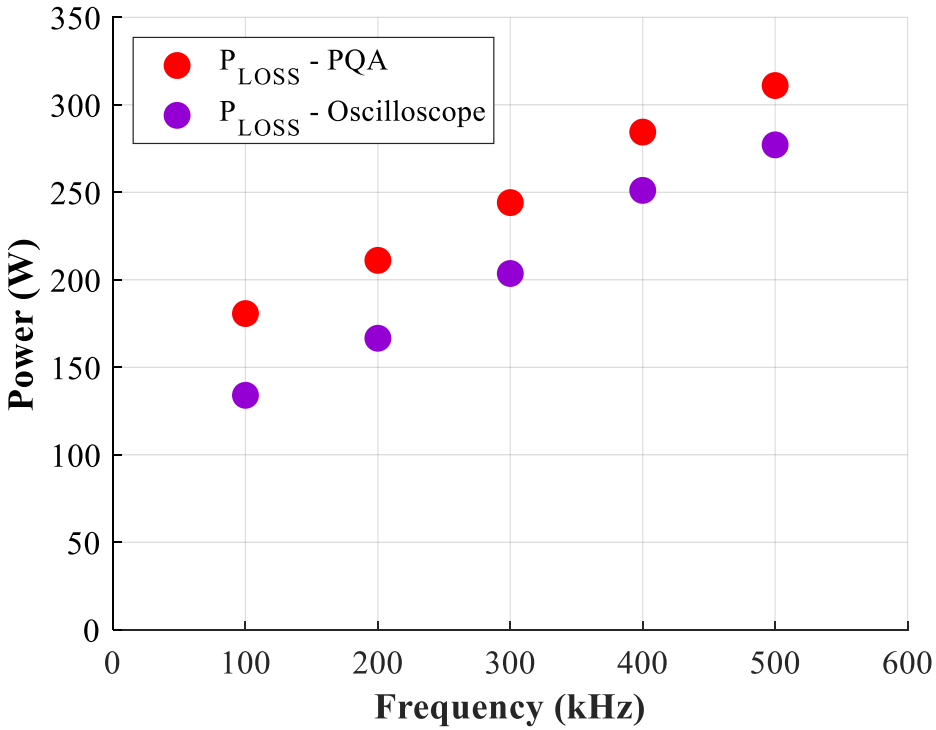


Figure 42: Raw power loss results from CCO using PQA and oscilloscope

The first observation about the data shown in Figure 42 is that both metrology configurations produce a loss-vs.-frequency plot that appears linear. To quantify the linearity of these results, linear regression was applied to both datasets using the least-squares method. The fitted linear trends for both datasets are shown in Figure 43, along with the corresponding coefficients of determination (R^2). Visual inspection of this plot suggests that a linear trend is a reasonable approximation for both datasets; and the computed R^2 values corroborate this visual analysis. This result is also consistent with the findings reported in [49].

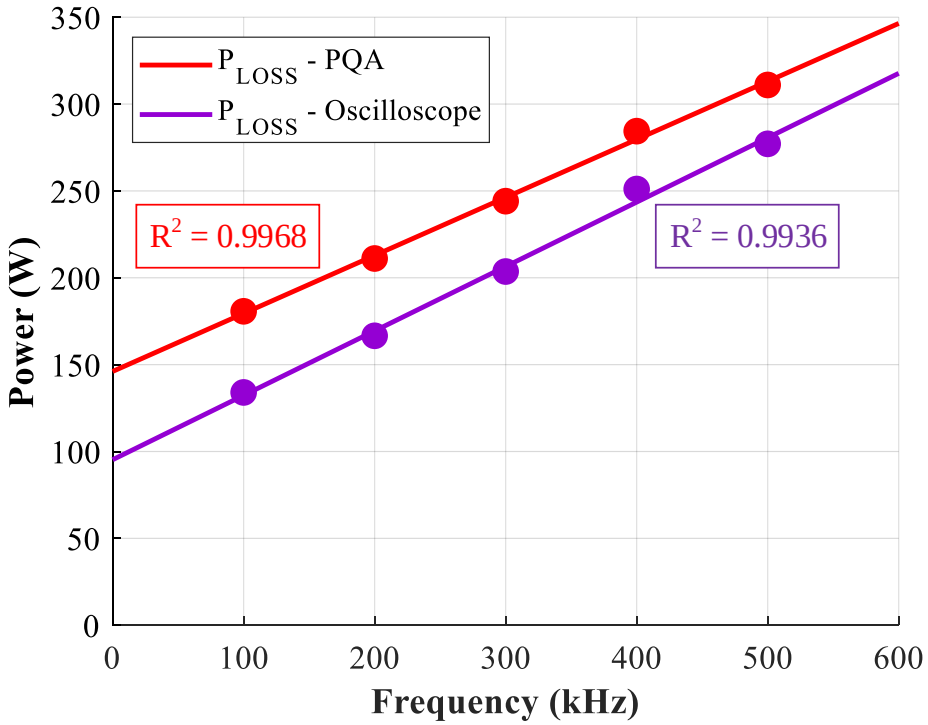


Figure 43: Raw power loss results from CCO with linear fit lines

The confirmed linearity of these results facilitates the separation of the losses into frequency-independent and frequency-dependent losses. This is realized by subtracting the y-intercept of the linear fit from both the trendline and the data points. The resulting loss values with the frequency-independent components removed is shown in Figure 44. This analysis does not suggest that the converter could actually operate at a switching frequency of 0 Hz. However,

since conduction losses are assumed to remain approximately constant across switching frequencies, this tool allows for the separation of the conduction losses without knowing the specific details about the dissipative elements in the circuit.

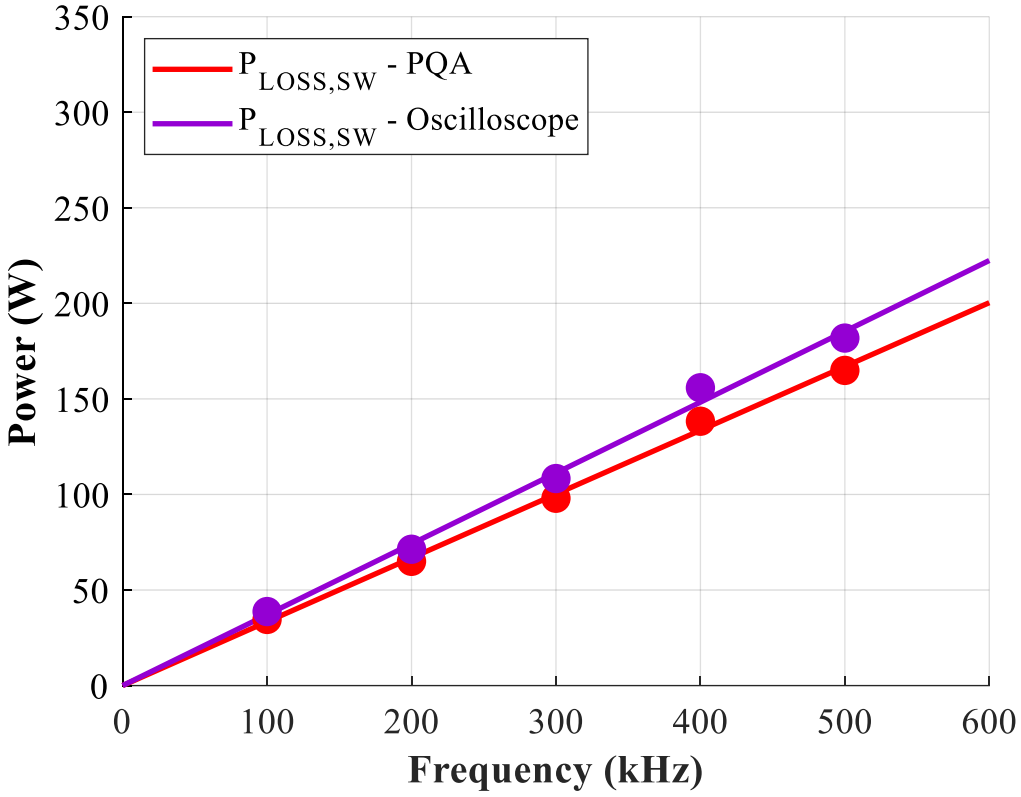


Figure 44: Frequency dependent CCO losses

By observing the slope of the trendlines in Figure 44, switching loss estimates can be made as discussed in Section 3.1. The switching loss estimates computed for both metrology configurations under consideration are shown in Table 4. Note that only the total switching loss values (E_{SW}) are shown since the CCO technique does not support the separation of switching loss into individual turn-on and turn-off energy values.

TABLE 4: CCO SWITCHING LOSS ESTIMATIONS

	E_{SW} (μJ)
PQA	333.9
Oscilloscope	370.7

Another important observation from Figure 42 is that the oscilloscope consistently produces lower power loss estimates than the PQA for the same system under identical conditions. This difference is further corroborated by Table 4, which shows that the oscilloscope estimates higher frequency-dependent losses than the PQA. One reason for this difference is the length of time that the data is averaged in the two metrology configurations. To demonstrate the influence of averaging time, Figure 45 shows five minutes of power loss data logged by the PQA while the converter was operated at 100 kHz. Although the plot is focused on a small section of the y-axis, it indicates that the total power loss value is not constant during the duration of the experiment. Based on the maximum and minimum power loss values shown in this plot, if only a single data point was recorded at each operating frequency (instead of logging the data over time), the recorded power loss could include an error of more than 5.0 W (3%). It should also be noted that the data presented in Figure 45 is actually averaged internally by the PQA using an unknown algorithm before it is recorded. Thus, the error in the oscilloscope-measured loss values could include significantly greater error than predicted by this example. Therefore, the oscilloscope loss estimates are expected to be less accurate than the PQA estimates because the considered waveforms are averaged over a significantly shorter duration compared to the PQA.

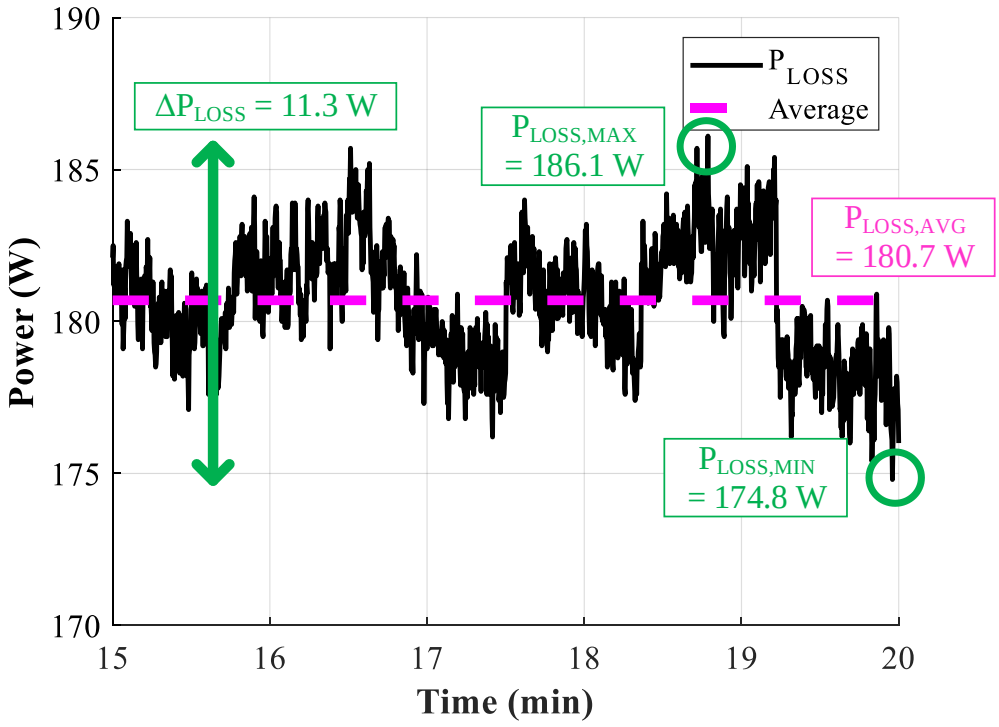


Figure 45: PQA power loss during CCO at 100 kHz switching frequency

In this work, the oscilloscope data was averaged over five seconds of converter operation instead of measured at a single sample. This averaging is expected to improve the fidelity of the measurements compared to a single sample. However, it is unlikely that this averaging operation could reach the same level of accuracy as the PQA measurements. To understand the potential error introduced by the reduced averaging window, a 25-point moving average was applied to the logged PQA data. Since the sampling period of the PQA is 0.2 seconds, 25 points of data is equivalent to averaging across five seconds (the duration of the oscilloscope measurements). The moving average of the PQA loss data is shown in Figure 46. Comparing the minimum and maximum of this data to Figure 45 indicates that the five second averaging does improve the variation in the results, but it is still possible for the oscilloscope to estimate losses that differ significantly from the long-term average value.

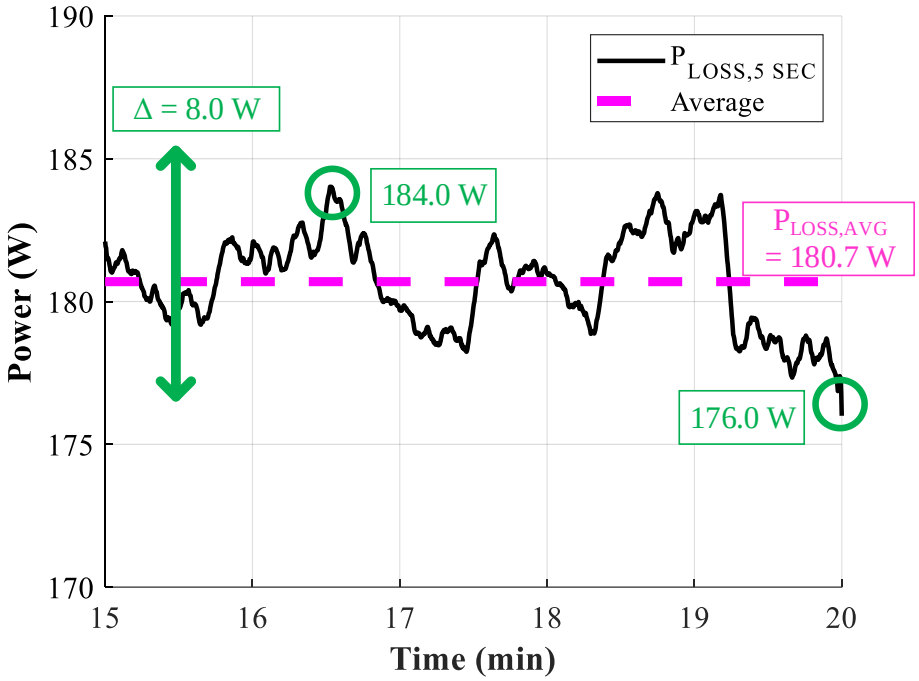


Figure 46: PQA power loss with five-second moving average

The measurements shown in Figure 42 differ by a larger amount than can be justified by the discrepancy in averaging time alone. If the averaging window justified the entire difference in data, then the oscilloscope-derived loss values at 100 kHz would fall within the range of values shown in Figure 46. However, the oscilloscope-derived power loss value is 40 W lower than the minimum PQA data point at 100 kHz. A comparison of the range of captured PQA loss values and the oscilloscope-derived loss value is shown in Table 5. At other switching frequencies, the oscilloscope-derived power loss value also falls outside the PQA bounds.

TABLE 5: COMPARISON OF PQA POWER LOSS AND OSCILLOSCOPE-DERIVED POWER LOSS

	P_{LOSS} (W)
PQA	176.0 - 184.0
Oscilloscope	134.0

In order to understand the reason for this discrepancy, it is important to recognize that it is challenging to accurately measure high-amplitude dc current. As discussed in Chapter 2, this is challenging due to the high-frequency content present in the captured waveforms as well as potential thermal considerations with current sensors and other instrumentation. Potential inaccuracies with the oscilloscope metrology can be evaluated by referencing the instrument specifications. The accuracy specifications for each of the instruments under consideration are summarized in Table 6 in terms of maximum percent error for voltage and current [50], [51]-[71]. There are three points about these specifications that should be noted. First, these specifications are only for dc measurements; the results differ significantly when evaluating converter dynamics. Second, the instrument literature specifies error percentages relative to the expected magnitude of the measurements. Therefore, the values shown in this table are calculated based on the operating conditions of the converter under consideration and are not universal for all measurement ranges. Please refer to the Appendix for further details regarding the computation of the values shown in Table 6. Third, the specified oscilloscope accuracy values only include error due to the probes; these values do not include the additional error induced by the oscilloscope itself.

TABLE 6: MAXIMUM DC PERCENT ERROR OF CCO METROLOGY

	Current	**Voltage**
PQA	$\pm 0.326\%$	$\pm 0.23\%$
Oscilloscope	$\pm 1.0\%$	$\pm 2.2\%$

Even without considering the additional error contributed by the oscilloscope itself, the oscilloscope error is significantly greater than the PQA error for these high-power, low-bandwidth measurements. The reason for this is difference is that the PQA is designed specifically for low-frequency measurements; whereas the oscilloscope and associated probes are

designed to balance the trade-offs between accurately measuring both low- and high-frequency signals. When these errors are considered in the measurements, the oscilloscope estimation can vary significantly as shown in Table 7. The table shows the minimum and maximum power loss for the PQA and oscilloscope at 100 kHz when the error of the instrumentation is considered. This implies that the oscilloscope metrology is not ideal for determining the efficiency of converters during normal operation. Due to the error introduced in the oscilloscope measurements, for the remainder of this work, only the PQA measurements from the CCO tests will be used for comparisons.

TABLE 7: COMPARISON OF PQA AND OSCILLOSCOPE POWER LOSS RANGES

	$P_{LOSS,MIN}$ (W)	$P_{LOSS,NOM}(W)$	$P_{LOSS,MAX}$ (W)
PQA	142.8	180.7	218.6
Oscilloscope	-97.8	134.7	365.8

6.2. Double-Pulse Test Results

Five DPT experiments were performed at the operating condition of interest – 20A, 600 V. An example set of waveforms for one of these tests is shown in Figure 47(a) for the turn-off event and Figure 47(b) for the turn-on event.

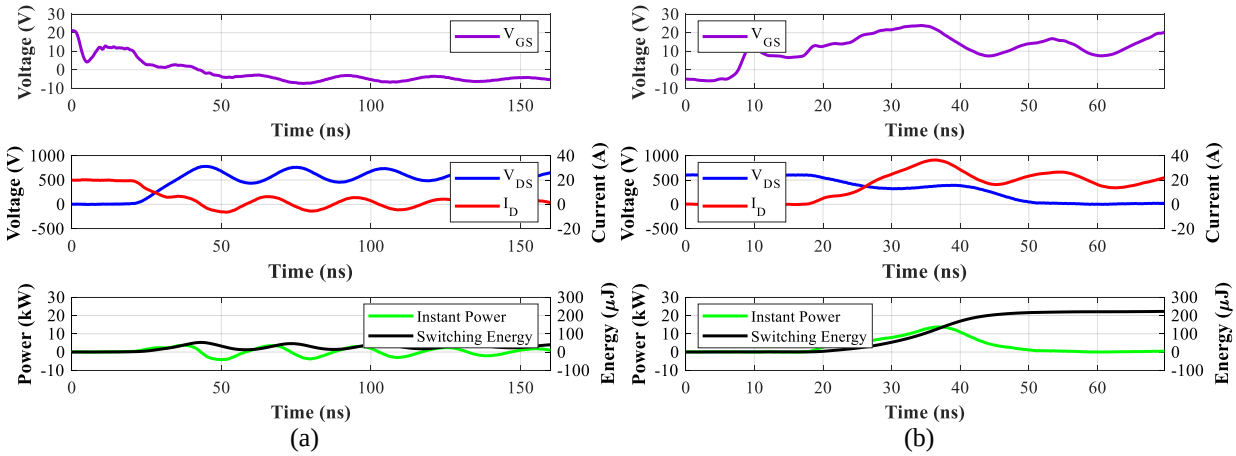


Figure 47: Example DPT results for (a) turn-off and (b) turn-on

The switching energy loss during both transitions was determined for each of the five experiments by integrating the instantaneous power waveform across the duration of the switching event. The limits of integration for the turn-on event were selected to capture the instantaneous power loss spike, and the limits of integration for the turn-off event were selected to capture the initial four oscillations in the instantaneous power. The loss estimates for each of the five DPT experiments are shown in Figure 48. Across all five experiments, the switching loss estimates are in good agreement. The results from these five experiments were averaged to obtain a single switching loss estimate for the DPT approach, which is provided in Table 8.

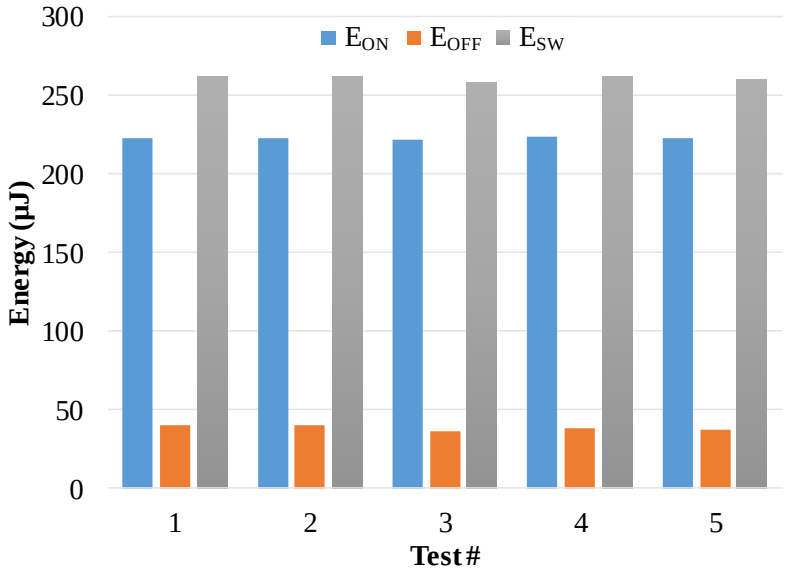


Figure 48: Individual DPT switching loss estimations

TABLE 8: AVERAGED DPT SWITCHING LOSS ESTIMATION

Event	Energy (µJ)
E_{ON}	222.8
E_{OFF}	38.4
E_{SW}	261.2

6.3. Comparison of Loss Techniques

Based on the results presented in the previous sections, a comparison of the switching loss estimates for the CCO and DPT techniques can be performed. The total switching loss estimates for both techniques are summarized in Table 9.

TABLE 9: LOSS ESTIMATES

Technique	E_{SW} (μJ)
CCO	333.9
DPT	261.2

Visually, this relationship can be illustrated by plotting the CCO frequency-dependent losses and the predicted DPT losses at each frequency on a loss-vs.-frequency plot. Such a plot is shown in Figure 49. This plot does not suggest that the DPT procedure was carried out at various frequencies, since DPT experiments are switching-frequency independent. Instead, the DPT line in Figure 49 demonstrates the predicted average switching power loss of the DUT during continuous operation using DPT-estimated losses. This prediction is created by multiplying the switching frequency by the DPT loss estimate shown in Table 9.

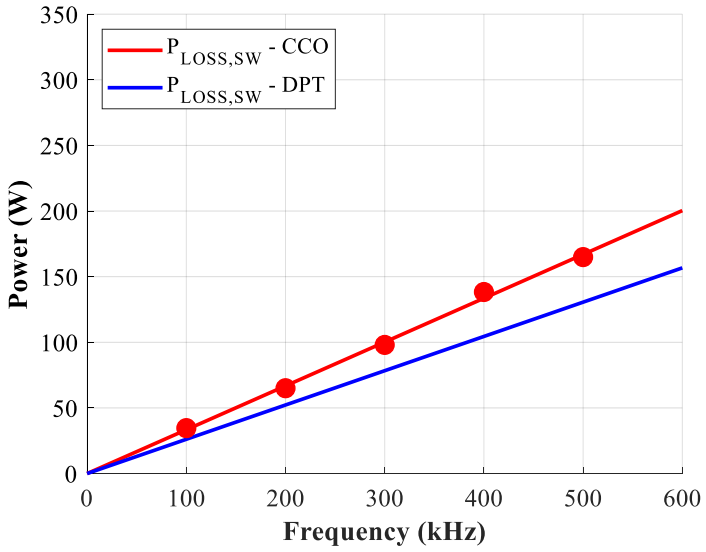


Figure 49: Frequency dependent loss comparison – CCO and DPT

From Table 9 and Figure 49, it is observed that the switching loss estimate from CCO is 27.8% higher than the switching loss estimate from DPT. This difference is believed to result from one of the underlying assumptions of the CCO technique. Specifically, the assumption that all frequency-dependent losses in the converter result from the switching action of the DUT may not be valid in this case. As described previously, there are other frequency-dependent loss mechanisms in most converter topologies that can potentially influence these results. For the boost converter used in this work, the most notable of these loss mechanisms is the contribution from the diode. In this implementation, a Schottky diode is utilized to eliminate reverse recovery losses, but the diode still has capacitive losses. These losses are typically much smaller than the reverse recovery losses for a PN-junction diode, but they may not be negligible. When using a PN-junction diode, these capacitive losses are not separable from the reverse recovery losses. However, in the case of the Schottky diode, the capacitive losses can be quantified separately. These losses can be estimated by Equation (18):

$$P_{diode,CL} = Q_C \cdot V_{d,neg} \cdot f_s \tag{18}$$

where $P_{diode,CL}$ is the diode loss due to capacitive recovery, Q_C is the diode's total capacitive charge at the blocking voltage, $V_{d,neg}$ is the voltage blocked by the diode, and f_s is the switching frequency. In a boost converter, the diode blocks the output voltage, which is 600 V in this setup. The capacitive charge is a function of the input voltage, which is held constant for all experiments described in this work. The value of the capacitive charge can be extracted from the diode datasheet. Switching frequency is the only value in Equation (18) that does not remain constant over the operating conditions considered in this work. Therefore, it is expected that the diode capacitive recovery loss should scale linearly with the converter's switching frequency. When the diode capacitive recovery loss is added to the DUT switching loss estimate obtained

from DPT, the resulting combined loss trend agrees more closely with the switching loss estimate obtained from CCO. The combination of the diode capacitive recovery loss and the DUT switching loss estimate obtained from DPT are compared to the switching loss estimate from CCO in Figure 50.

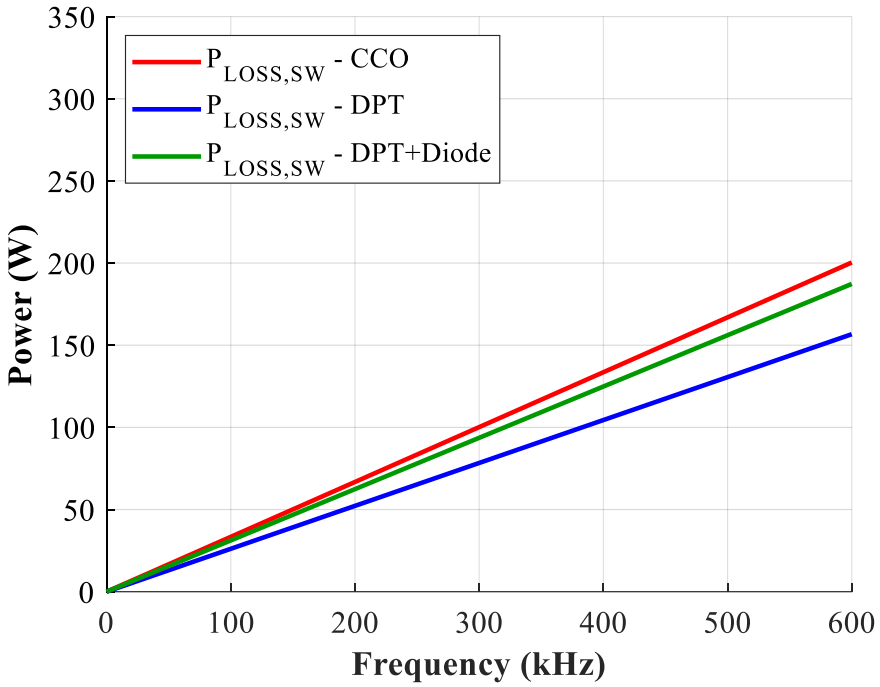


Figure 50: Frequency dependent loss comparison – CCO and DPT with diode

It is important to note that the results of Figure 50 are not intended to demonstrate perfect agreement between the CCO and DPT techniques. However, this figure illustrates that the CCO technique is not able to cleanly isolate the switching losses of the DUT. Instead, the contribution of other frequency-dependent loss mechanisms are included in the estimate. In this instance, it is clear that the diode capacitive recovery losses must be removed from the CCO measurements to obtain a more accurate switching loss estimation for the DUT. However, even if the diode capacitive recovery losses are removed, there are additional losses that must be also removed before the CCO estimates would accurately represent the switching loss of the DUT. These

additional loss mechanisms, specifically core losses and high-frequency ohmic losses, are difficult to model accurately due to challenges such as the dependence on curve fitting empirical data and the influence of dc bias [72]-[73]. These difficulties with estimating additional converter losses accentuates the challenge of trying to isolate DUT losses using CCO.

6.4. Analysis of the Results

First, it can be concluded from this work that an oscilloscope is not the proper instrument to employ for estimating switching losses using the CCO technique. This also implies that this metrology is not ideal for determining the efficiency of converters during normal operation. The oscilloscope's design balances the need for accuracy in both low- and high-bandwidth measurements. As such, this trade-off leads to reduced accuracy compared to the PQA when extremely low-bandwidth measurements are performed. Thus, the evaluation of power loss and efficiency in converters during continuous operation should be performed using a PQA whenever possible.

Second, by comparing the losses measured with the CCO and DPT techniques, it is determined that the CCO technique consistently estimates higher DUT switching losses than the DPT technique. This conclusion is not unexpected since the CCO technique assumes that all other frequency-dependent losses in the system are negligible in comparison of the DUT switching losses. The difference between the DPT and CCO cases confirms that the switching loss of the DUT is not the only significant frequency-dependent loss mechanism in the converter used in this work. If the losses predicted by the CCO technique are assumed to be solely attributed to the switching loss of the DUT, this quantity would be over-estimated by 27.8% on average. The difference between the CCO and DPT estimates can be attributed to the frequency-dependent losses of the diode, inductor core losses, and the temperature dependence of various

components in the system. This claim is verified in this chapter by adding the predicted loss contribution from the diode to the DUT switching loss obtained from DPT to obtain improved agreement between the CCO and DPT estimates. This suggests that the CCO estimates include losses from the DUT, diode, as well as additional loss mechanisms that have not been identified. Overall, this finding suggests that the DPT procedure provides a more accurate estimate of DUT switching losses than the CCO procedure.

CHAPTER 7:

CONCLUSION

The goal of this thesis is to compare two of the most widely used techniques for estimating switching losses of power semiconductors: CCO and DPT. This thesis evaluated both of these techniques in terms of accuracy, ease of implementation, and metrology considerations. An empirical test platform was designed and fabricated to evaluate these techniques with minimal changes required to the setup between the techniques. The same DUT was evaluated with both techniques utilizing essentially the same circuit, and the resulting switching loss estimations were compared. It was found that the CCO technique over-estimates the DUT switching losses by 27.8% compared to the DPT technique, on average. The discrepancy between the two techniques can be attributed to the frequency-dependent loss contributions of the diode, inductor core losses, and the temperature dependence of various components in the system. This corroborates claims found in the literature that the CCO technique is not able to isolate the switching loss of the DUT, and suggests that the DPT procedure provides a more accurate estimate of DUT switching losses than the CCO procedure

7.1. Proposed Future Work

This section addresses potential future extensions of this work. One immediate extension of this work would be to perform similar comparisons with different semiconductors operating at varying loads to evaluate the CCO and DPT techniques at different operating conditions. Acquiring additional data would serve multiple purposes. First, additional data could be used to further validate the claims already made in this thesis. Second, the observed discrepancies

between the CCO and DPT measurements could be used to generate rules-of-thumb for the magnitude of error in CCO switching loss estimations. This could give insight to designers who need to estimate switching loss more accurately than is possible with CCO, but who do not have access to the metrology and purpose-built hardware necessary for DPT evaluation.

Another possible extension of this work would be to evaluate the switching loss estimations from the calorimetric and opposition techniques discussed in Section 1.3. Adding these additional techniques to the comparison would broaden the scope of this work and improve confidence in the accuracy of the resulting estimations.

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APPENDIX

The PQA dc voltage accuracy is defined as "±0.05% of reading ±0.1% of range ± 0.05 V" [50]. The two voltages measured by the PQA were 600 V (V_{OUT}) and ~340 V (V_{IN}) which are measured in the 1000 V and 500 V ranges, respectively. Equations (19) and (20) show the calculated absolute voltage error for each of these measurements, and Equations (21) and (22) show the percent error.

$$V_{error,Vout} = 600 \cdot 0.0005 + 1000 \cdot 0.001 + 0.05 = 1.35\ V \tag{19}$$

$$V_{error,Vin} = 340 \cdot 0.0005 + 500 \cdot 0.001 + 0.05 = 0.72\ V \tag{20}$$

$$Error_{Vout} = \frac{1.35}{600} = 0.23\% \tag{21}$$

$$Error_{Vin} = \frac{0.72}{340} = 0.21\% \tag{22}$$

The PQA dc current accuracy is defined as "±0.05% of reading ±0.1% of range ± (50 µV / Z_{ext})" [50]. For the 30 A internal current shunt used for the all the measurements in this work, Z_{ext} is 9.375 mΩ. The two currents measured by the PQA were ~11 A (I_{OUT}) and 20 A (I_{IN}) which are measured in the 20 A and 50 A ranges, respectively. Equations (23) and (24) show the calculated absolute voltage error for each of these measurements, and Equations (25) and (26) show the percent error.

$$I_{error,Iout} = 11 \cdot 0.0005 + 20 \cdot 0.001 + \frac{50 \times 10^{-6}}{0.009375} = 0.0308\ A \tag{23}$$

$$I_{error,Iin} = 20 \cdot 0.0005 + 50 \cdot 0.001 + \frac{50 \times 10^{-6}}{0.009375} = 0.0653\ A \tag{24}$$

$$Error_{Iout} = \frac{0.0308}{11} = 0.28\% \quad (25)$$

$$Error_{Iin} = \frac{0.653}{20} = 0.326\% \quad (26)$$

The maximum percent error from this analysis for voltage and current measurements were used in Section 6.1 when comparing the PQA with the oscilloscope for CCO measurements.