

SOLUTION-PROCESSED DOPING

IN CdTe THIN FILM SOLAR CELLS

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ABSTRACT

Cadmium Telluride (CdTe) is one of the leading photovoltaic (PV) technologies in the world with a world record $\sim 22.1\%$. With a bandgap of 1.45eV and a high absorption coefficient, the theoretical power conversion efficiency limit of 32% is limited by recombination and high resistivities in CdTe devices. Doping CdTe is a necessary way to improve device performance. In this work, it is demonstrated that a cost-effective solution-processed Group I and Group V doping in CdTe thin film solar cells allows for efficiency increases and stability improvement in CdTe devices. By varying the doping concentration, activation annealing temperatures, and deposition parameters, the root cause for the increased power conversion efficiency was investigated. Group I and Group V dopants showed smoother films indicating less resistance through the back contact leading to an increase in power conversion efficiencies, PCE%.

Structural properties were investigated using Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM) and X-ray Diffraction (XRD). Electrical characterization of completed devices was carried out using Current-Voltage (I-V), External Quantum Efficiency (EQE) and power conversion efficiency (PCE%).

This work systematically investigated the extrinsic doping to improve the CdTe device performance in an affordable means to integrate into the CdTe thin film solar module manufacturing. The achievement could be used to further reduce the cost of solar energy.

DEDICATION

I dedicate this dissertation to my parents, S. and D. Montgomery, my stepmother A. Montgomery, my sisters, brother, nieces, and nephew. And to you my love, who continues to supports my every mission.

LIST OF ABBREVIATIONS AND SYMBOLS

μm	Micrometer
nm	Nanometer
α	Absorption Coefficient
$^{\circ}$	Degree sign
λ	Wavelength
CB	Conduction Band
VB	Valence Band
CBM	Conduction Band Minimum
VBM	Valence Band Maximum
S-Q Limit	Shockley-Quisser Limit
SRH	Shockley-Read-Hall Recombination
V_{bi}	Built in Potential
CdTe	Cadmium Telluride
CdZnTe	Cadmium Zinc Telluride
CdS	Cadmium Selenide

CdCl ₂	Cadmium Chloride
AX	Acceptor Type Compensating Defects
DX	Donor Type Compensating Defects
TCO	Transparent Conductive Oxide
TEC15	Flourine Doped SnO ₂ Coated Soda Lime Glass
GaAs	Gallium Arsenide
CIGS	Copper Indium Gallium Selenide
DSSC	Dye-Sensitized Solar Cells
PVSC	Pervoskite Solar cells
STC	Standard Test Conditions
η	Power Conversion Efficiency PCE %
V_{oc}	Open-Circuit Voltage
V_{MP}	Voltage at Maximum Power
J_{sc}	Normalized Short-Circuit Current
J_{MP}	Current at Maximum Power
I_{sc}	Short-Circuit Current
MPP, PMax	Maximum Power Point
C-V	Capacitance-Voltage

I-V, J-V	Current-Voltage
FF	Fill Factor
P_{in}	Input Power
R_S	Series Resistance
R_{SH}	Shunt Resistance
N_A/N_D	Acceptor/Donor Doping Concentration
KT/q	Thermal Voltage
Δn	Excess Carrier Concentration
<	Less than
n_i^2	Intrinsic Carrier Concentration
Si	Silicon
Cu	Copper
CuSCN	Copper (I) Thiocyanate
Ag	Silver
AgSCN	Silver (I) Thiocyanate
As	Arsenic
$AsCl_3$	Arsenic Trichloride
Sb	Antimony

SbCl ₃	Antimony Trichloride
E _g	Bandgap
PV	Photovoltaic
SEM	Scanning Electron Microscopy
AFM	Atomic Force Microscopy
EFM	Electrostatic Force Microscopy
XRD	X-ray Diffraction
UV-Vis	Ultra Violet Vi
CBD	Chemical Bath Deposition
EQE	External Quantum Efficiency
CO ₂	Carbon Dioxide
IPA	Isopropyl Alcohol
DES	Diethyl Sulfide
NH ₄ OH	Aqueous Ammonium Hydroxide

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CHAPTER 1

INTRODUCTION

1.1 Motivation

Renewable energy has been a significant interest for scientist trying to answer concerning questions on economic changes for the present day compared to the past and for the decades to come. The dependence on burning fossil fuels for conventional means is the main cause of the greatest man-made environmental challenge on Earth, climate change¹. Greenhouse gas emissions absorb thermal radiation emitted from the Earth's surface resulting in increased amounts of warming in the atmosphere which sets the course for the undesirable global warming¹

During the ice age, CO₂ levels were around 200 parts per million (ppm), now as of Summer of 2019, the world just passed the symbolic 415 parts per million (ppm) threshold of CO₂ concentration making this temperature the hottest year on record¹ and it is assumed to continue to increase to 1500 ppm in future years. Concentration of CO₂, methane, soot, and other pollutants release into the atmosphere and act as a blanket, trapping the suns heat and causing the planet to warm^{1,2}. Research shows that the production of electricity using coal, petroleum and other uses of fossil fuels affect the environment in ways that we did not understand before. As the temperature worsens, many types of disasters, including storms, heat waves, floods and droughts warm the climate creating an atmosphere that can collect, retain and drop more water³. In this event, a change weather patterns in such a way that wet areas become

wetter and dry areas become drier will occur. Furthermore, glaciers, which were once in filled with aged thickened snow mass, are often used as indicators of climate change⁴. In the past 200 years or so, heat trapping gases related to the cause of global warming are known to be the cause of glacier retreats. When the melting of a glacier exceeds the growing of snow, a glacier retreat occur⁵. This retreat happens when the snow mass does not extend as far down valley as it once previously did which results from ice melting more quickly than snowfall can accumulate. Higher temperatures and less snowfalls cause many glaciers around the world to retreat. In addition, the increasing number of droughts, intense storms and floods reports which results catastrophic failure and more importantly, public health and safety⁶. Fresh water shortage is another big challenge to humanity as the global population and detrimental natural causes continue to increase. Currently, about 40% of the global population – approximately 663 million people on our planet lack access to safe, clean drinking water; 700 million people in 43 countries are affected by water scarcity, particularly in the Middle East and North Africa⁷.

As climate change and the burning of fossil fuels continue to increase, complex relationships between world development and water demand for countries and regions that are without the essential need of fresh water due to critical national water-stress problems will continue to become difficult to resolve⁸. By 2025, 1.8 billion people are expected to be living in countries or regions with absolute water scarcity⁸. By 2030, 24 million and 700 million people will be affected and two-thirds of the world population could be under water-stress conditions^{9, 10} leading to a volumetric increase of water scarcity in regions around the world lacking physical water resources, water quality and water accessibility which undoubtedly leads to increased health risks with all people on earth.

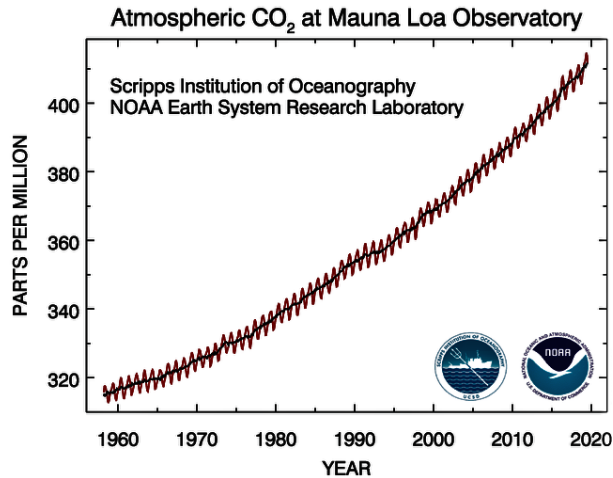


Figure 1: Shows CO₂ data measurements from Mauna Loa, the longest record of direct CO₂ measurements¹¹

Figure 1 shows carbon dioxide data measurements in dry air on the constitute of Mauna Loa where lies the longest record of direct measurements of CO₂ in the atmosphere since 1958. This figure shows how the increase in heat trapping CO₂ levels are expected to continue to increase by 2020 leading to a national crisis such as respiration and volcanic eruptions¹².

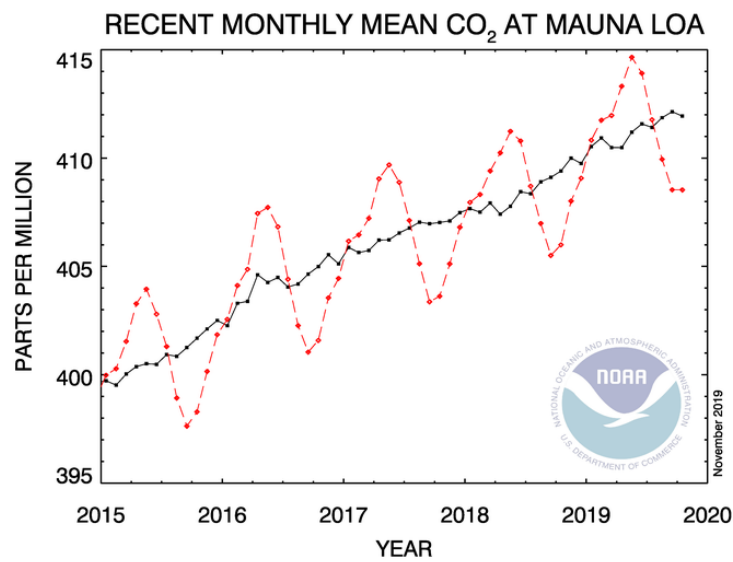


Figure 2: CO₂ Concentration levels rising past 400 parts per million¹³

In fact, as Figure 2 shows, as of May 2019, we are near the annual peak of atmospheric disaster as the concentration of CO₂ is unmistakably at the highest level it has been in the last two million years¹⁴. In fact, climate change is affecting all of us here and now. Even if we opted out of greenhouse caused circumstances, the impacts would not disappear, CO₂ levels in the atmosphere will stay for thousands of years or more^{6, 15}.

1.2 Photovoltaic (PV) history

The photovoltaic effect was first seen in 1839 however; scientist did not discover how it worked until 1954¹⁶⁻¹⁸. A photovoltaic system uses solar panels to capture incident sunlight photons and when exposed to the device, an electric potential or direct current (DC) in semiconductors is produced with enough energy to promote the electrons to excite from the valence band to the conduction band. The word "photovoltaic" derived from the Greek meaning light, and voltaic comes from the name of the Italian physicist Volta¹⁹. If the incoming photon has enough energy when exposed to the p-i-n junction of the solar cell, this energy will promote the electrons/hole to excite from the valence band -to conduction band producing an extra electron or from the conduction- to valence band producing a hole where both participate in conduction. In the 1970's, improvements in manufacturing, performance and quality of PV modules helped to reduce the costs associated with the fabrication of modules which opened up a number of opportunities for powering remote terrestrial applications like satellites, battery charging for navigational needs, signals, telecommunication equipment and other critical, low-power needs²⁰ Today, the industry of PV modules continues to rapidly grow in major cities all over the world including U.S., Japan, Europe, China, Australia, Germany, South Korea and India leading to a new age of PV systems integrated into building and interconnected to utility networks providing solar power to a large range of end-users.

1.3 Photovoltaic (PV) cost

Incorporating PV technology as a renewable energy source is reliable with limited maintenance cost during its operation, PV is also environmentally friendly and proves its effectiveness through increase power conversion efficiencies¹⁸. However; in order to enhance long term commercialization, low fabrication cost is necessary for continued PV market growth²⁰. Since the 1970s, R&D in this area has been driven by performance and improvements within this technology has demonstrated stable commercialization.

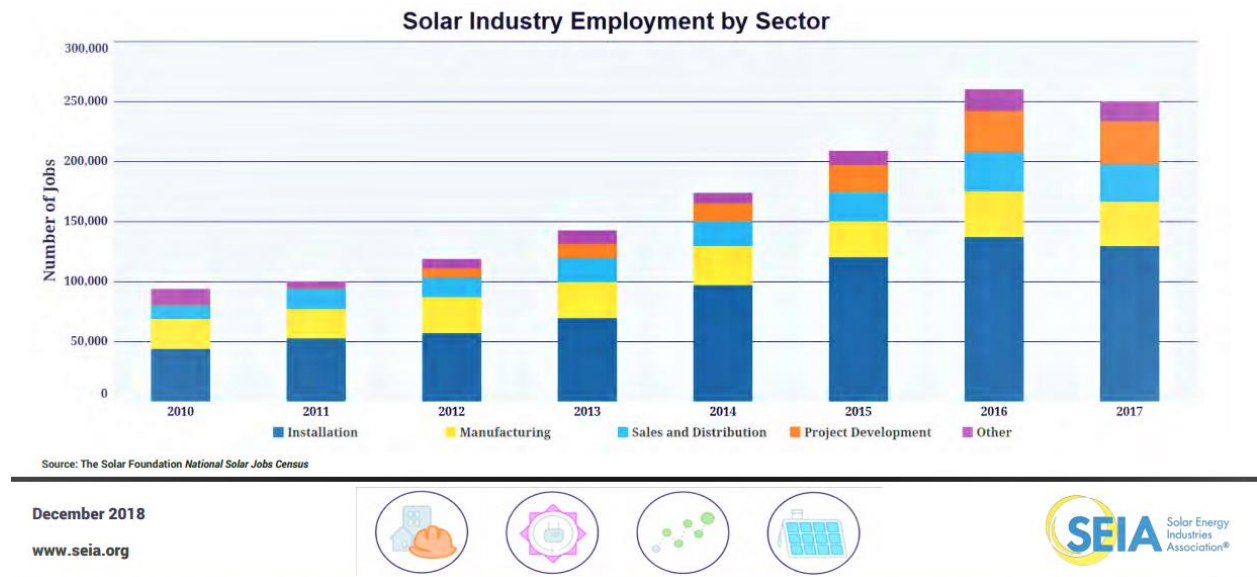


Figure 3: Historic development and solar PV power generation national target (SEIA)

Figure 3 from the Solar Energy Industries Association (SEIA) shows that the cost to install solar has dropped by more than 70% over the last decade, leading to an expansion of new markets^{21, 22}. This report shows lowest levels in history across all market segments. An average-sized residential system has dropped from the pre-incentive price of \$40,000 in 2010 to roughly \$18,000 today, while recent utility-scale prices range from \$28/MWh - \$45/MWh which is competitive for all other generations²³. In addition, other reports show solar PV technology has

increased at a rate of 40% growth in power generation within the past couple of years with an average annual growth of 17% between 2017 to 2030 which is the highest-ranking renewable energy source estimated by the International Energy Agency (IEA)²⁴. As PV cost continues to decline, PV electricity will be able to compete directly with retail electricity rates in rooftop solar markets and wholesale electricity rates in utility solar markets²². Since the fabrication of PV modules consumes energy, some may question its effectiveness at the reduction of CO₂ emissions.

However, it must be recognized that the stimulation of government incentives and subsidies has played a major role on the impact of decision making for the consumer. Some countries have increased PV installation growth tremendously compared to the US by allowing government subsidies for the consumer. This direct benefit has shown a remarkable growth in PV installations but has decreased recently due to the cut down of subsidies²⁵. First Solar, the worlds largest thin film CdTe PV manufacturer, has reduced the CdTe module manufacturing cost from \$1.02/W in 2010 to less than \$0.45/W in 2017 from large R&D investments^{22, 26}. By 2017, First Solar has increased their cell and module efficiencies from 16.5% to 22.1% and from 14.4% to 18.6% respectively²⁷. Overall, the increase in the performance of PV technologies has improved substantially over the years, and much of that credit is due to technical innovation with new and improved materials in addition to improved PV manufacturing processes by more simple cost effective measures. These factors contribute to an increase PV demand coupled with a downward trend in PV pricing concludes rapid growth within the PV market.

1.4 Photovoltaic technologies

1.4.1 First-generation wafer PV

PV technologies can be classified into three main categories, the first generation wafer based solar cell, the second generation thin film based solar cell and the emerging third generation solar cell technology.

The efficiency of the first reported Si solar cell was 6%². Since then, substantial advancements have been made and current efficiencies have reached 26.3% for a single junction cell and 22.4% for large area modules³. Today, crystalline silicon technologies constitute about 90% of the current PV market with an expected lifetime of 25 years²⁸. Standard architecture for crystalline silicon dominates the market today but non-standard architectures like tandem cells and all inorganic perovskite architectures are growing rapidly in the market importance due to their ability to offer higher efficiencies. In fact, expensive standard crystalline silicon technologies have efficiencies of 26.7%²⁹ while non-standard crystalline architectures have achieve a module efficiency of up to 20.9%³⁰.

Si solar cells can be classified as single crystalline or multi crystalline. Mono (single) crystalline, as the name indicates, are made from single crystals of silicon (Si). The cells are then sliced from large crystals grown under controlled conditions³¹. Multi-crystalline (polycrystalline) Si are composed of randomly oriented grains with grain boundaries that produce defect sites for e-h pairs to recombine and stop conducting. Current record efficiencies for monocrystalline are at 26.7% for small area cells and 10.5% for large area modules²⁹. Si has an indirect bandgap and therefore a low absorption coefficient, μ . The absorption coefficient determines how far incident light of a certain wavelength can penetrate material before being absorbed. A low μ would not be ideal for efficient conversion of light into electricity. In order to compensate these limitations, a very thick layer of the Si wafer is needed to absorb most of the incident light. Typical wafer thicknesses are about 100 – 300 μm which

adds to the high processing cost of Si which increases the overall price of the module⁵. In crystalline Si solar cells, the cost of Si constitutes to 40% of the final module price⁶.

1.4.1.1 Gallium arsenide (GaAs)

GaAs is a direct bandgap semiconductor with a well-matched solar spectrum and has been coupled with strong absorption that has been led to efficiencies of 28.8% for small area cells and 24.1% for modules¹⁰. However, the high manufacturing costs for these cells have limited their usage in space applications and concentrated solar power cells. The most expensive component of these solar cells is the GaAs parent wafer, which is grown by epitaxy³². Recent advancements have reduced the costs by using a technique called epitaxial liftoff which creates very thin layers of GaAs from the parent wafer allowing the wafer to be used multiple times¹¹. The cost of this type of PV technology is high even when compared to single crystal Si solar cells. Presently, these cells are predominantly used in space applications and solar power applications where lenses and curved mirrors are used to focus on small areas.

1.4.1.2 Multi-junction

The use of multiple junctions can improve the efficiencies of the cells dramatically. Multiple junctions (also called tandems or sub cells) are stacked on the top of each other and each sub cell absorbs light from a specific region of the solar spectrum. The sub cells are arranged in such a way that the light is incident on the material with the largest bandgap³¹. The bandgaps of the chosen material decreases as light travels away from the point of incidence. The conversion efficiency increases with the number of sub cells³³. The maximum theoretical efficiency that can be obtained by a single junction cell is close to 33%³³. For a cell with 2 junctions, this limit increases to 54%, and for a theoretical infinite number of junctions, the limit reaches 86%³⁴. Semiconductors made of Al, Ga, In and N, P, As, Sb can form high quality

crystalline films with variable bandgaps leading to efficiencies up to 46% for a 4-junction solar cell¹³.

1.4.1.3 Amorphous si

Amorphous Si solar cells are typically deposited by plasma-enhanced chemical vapor deposition (CVD) at low substrate temperatures¹⁴. Amorphous Si is well used for low power applications such as calculators because they are prone to light-induced degradation^{35, 36}. These cells offer better absorption than crystalline Si, however; its larger bandgap (1.7-1.8eV) does not match the solar spectrum well¹⁴⁻¹⁵. As a result, these cells exhibit lower efficiencies. Their efficiencies are limited to 13.4% for a triple junction cell¹⁰ which is not encouraging for commercial scale manufacturing. Moreover, these solar cells are known to degrade upon exposure to light causing stability issues making it undesirable for commercial applications¹⁶. The leading PV technology is Si with a 90% of the industry market share¹⁷. The other wafer-based PV technologies are currently limited to space applications due to the cost involved in the manufacturing process.

1.4.2 Second-generation thin film PV

The remaining 10% of the PV market is constituted mainly by thin film solar cells. Thin film PV cells consist of very thin absorber layers with a typical range of a few microns which has a thicknesses of about 100 times thinner than crystalline silicon³⁷. The semiconducting layer in this research is deposited on a low cost substrate via a cost effective solution method which differs from the traditional vacuum deposition methods including dry methods used in other PV technologies.

An advantage, unlike the wafer-based cells, is that PV cells can be deposited on cheap substrates compared to wafer-based where cells need to be soldered together into strings and laid

out into a module³⁸. The semiconducting layer in this research is deposited on a low cost substrate via a cost-effective solution-based method which differs from the traditional vacuum deposition and dry methods used in other PV technologies. Thin film technologies include the following:

1.4.2.1 Cadmium telluride (CdTe)

CdTe is of primary focus during this research and is the leading thin film PV technology on the market today. With an ideal bandgap of 1.45 eV and a very strong absorption coefficient, CdTe is an ideal candidate for PV applications¹⁸. It offers the lowest module costs compared to any other PV technology on the market today³⁹. The toxicity of cadmium (Cd) and the scarcity of tellurium (Te) are concerns with respect to this technology. The current record efficiency of CdTe has surpassed the efficiency of multi-crystalline Si solar cells¹⁹.

1.4.2.2 Copper indium gallium selenium (CIGS)

Copper indium gallium selenium ($\text{CuIn}_x\text{Ga}_{1-x}\text{Se}_2$ or CIGS) are multilayer thin film components often deposited on cheap substrates. CIGS has and a large absorption coefficient and with a direct bandgap of 1.1-1.2 eV¹³. The voltage is improved making this technology attractive for many applications. The drawback in CIGS is in the expensive manufacturing tools needed to fabricate sufficient solar modules⁴⁰. CIGS is the most efficient of the thin film technologies⁴⁰, and although this technology has high efficiencies in the lab, the cost of commercial manufacturing has not yet been mastered²⁰. Like CdTe, CIGS solar cells show a better resistance to heat than silicon based solar panels^{21 41}.

1.4.3 Emerging third-generation thin film PV's

Emerging PV technologies employ nano-structured materials that can be engineered to achieve the desired optical and electronic properties. These technologies offer low cost fabrication that attract commercial scale production.

1.4.3.1 Dye-sensitized solar cells (DSSC) and perovskite (PVSC)

Emerging PV technologies employ nano-structured materials that can be engineered to achieve the desired optical and electronic properties. These technologies include: Dye-Sensitized Solar Cells (DSSC) and all inorganic perovskite or with the hybrid organic–inorganic lead halide architecture^{42, 43}. DSSC are considered to be the pioneer in the third emerging thin film market as far as technical maturity but perovskite is not far behind in PV technology⁴². DSSC's have achieved efficiencies up to 11.9% and 8.8% at the cell and module level respectively³⁷. However, the use of liquid electrolyte in DSSC causes problems with instability, risk of evaporation and a limited operating temperature which has all paved way for the innovation of perovskites^{42, 44, 45}.

Perovskites cells have evolved from DSSC's and is the fastest growing third generation PV technology achieving an efficiency up to 20.9% cell efficiency and up to 8.8% module efficiency in less than 3 years of their development⁴⁶. The term “perovskite” refers to the ABX_3 crystal structure, and the most widely investigated perovskite for solar cells is the hybrid organic–inorganic lead halide $CH_3NH_3-Pb(I, Cl, Br)_3$ architecture⁴⁷. This technology is in its early stages of commercialization and their further research is needed to ascertain stability.

1.5 Solar cell terminology

A current source in parallel with a forward biased diode can serve as the equivalent circuit of an ideal solar cell. Parasitic resistances such as series (R_S) and parallel (R_{SH}) resistances account for various loss mechanisms shown in Figure 4.

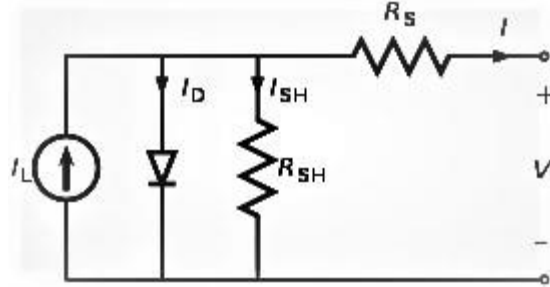


Figure 4: Equivalent circuit diagram of a solar cell⁴⁸

Resistive effects in a solar cell reduce the efficiency of the device by dissipating power in the resistances. Series (R_S) and parallel (R_{SH}) resistances are common parasitic resistance losses that impact the maximum efficiency collected in a solar cell device. The key impact of these losses reduce the fill factor of the device⁴⁷. Both the magnitude and the impact of the R_S and R_{SH} depend on the geometry of the solar cell. A common unit for resistance is in Ωcm^2 .

1.5.1 Conversion efficiency

The efficiency of a solar cell is the most common used parameter when comparing the performance of multiple solar cell devices. Efficiency is defined as the ratio of energy output from the solar cell to the input energy from the sun⁴⁹. Expressed as:

$$\eta = \frac{V_{OC} \times I_{SC} \times FF}{P_{in}} \quad (1)$$

Where, P_{in} is the power input from the sun.

V_{OC} is the open circuit voltage, I_{SC} is the short circuit current and FF is the fill factor. The efficiency depends on the solar energy spectrum, the intensity of the incident sunlight and the temperature of the solar cell⁵⁰. Conditions under which efficiency is measured must be carefully controlled in order to compare the performances of different solar cell devices. Fill factor, in conjunction of V_{OC} and I_{SC} , determines the maximum power from a solar cell. It is also

known as the “squareness” of the solar cell on the I-V curve in Figure 5 and is defined as the ratio of the maximum power to the product of V_{OC} and I_{SC} for the solar cell:

$$FF = \frac{V_m \times I_m}{V_{OC} \times I_{SC}} \quad (2)$$

Where, V_m and I_m are the voltage and current at maximum power points. The fill factor is a function of the series and shunt resistances of the solar cell. The FF shows the extent of electrical losses during the solar cell operation⁴⁹.

The short circuit current is the current through the solar cell when the voltage across the device is zero (when the solar cell is short circuited). The solar cell short-circuit is generally represented as current density, J_{SC} :

$$J_{SC} = \frac{I_{SC}}{A} \quad (mA/cm^2) \quad (3)$$

Where, A is the effective area of the solar cell. This parameter is a function of the solar illumination, optical properties and charge transfer probability of the solar cell⁵⁰. The open circuit voltage (V_{OC}) is the maximum output voltage available from a solar cell that occurs at zero current. The V_{OC} corresponds to the amount of forward bias on the solar cell due to its interaction with light-generated current. This is obtained when the cell is operating without a load (i.e. open circuited). It is a function of the semiconductor bandgap, doping concentration and charge recombination (minority carrier lifetime) of the cell⁵¹. The V_{OC} is given by:

$$V_{OC} = \frac{KT}{q} \ln\left(\frac{N_A + \Delta n}{n_i^2}\right) \quad (4)$$

Where KT/q is the thermal voltage, N_A is the doping concentration, Δn is the excess carrier concentration and n_i is the intrinsic carrier concentration.

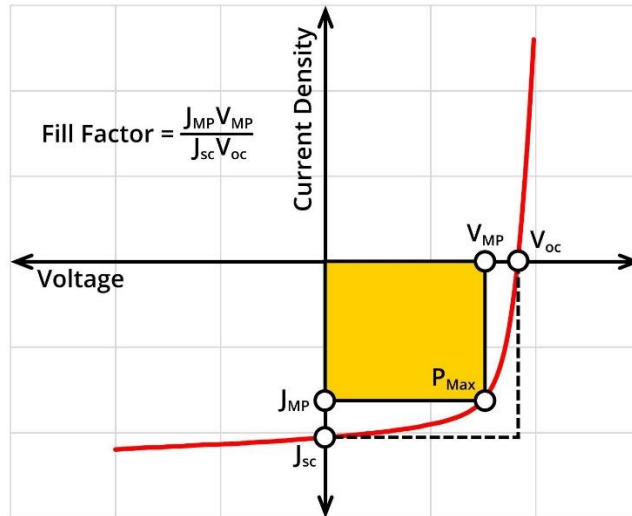


Figure 5: Typical current-voltage relationship of a solar cell⁴⁸

Figure 5 shows a typical current-voltage (I-V) relationship of a solar cell. The fill factor plotted using current density, highlighting the short circuit current density (J_{sc}), open-circuit voltage (V_{oc}), current and voltage at maximum power (J_{MP} and V_{MP} respectively), maximum point (P_{Max}) and fill factor (FF).

1.5.2 Solar spectrum and quantum efficiency

The performance in a solar cell depends on the incident light spectrum and intensity as well as the operating temperature. The solar spectrum changes daily and varies throughout the day. For reliable measurement of characteristics, it is vital to perform measurements under standard test conditions (STC). The internationally recognized standard condition for efficiency measurements for terrestrial applications is known as “AM1.5 Global” solar irradiation at a temperature of 25 °C. The total irradiance on the solar cell is 1000 W/m². This allows scientists to compare photovoltaic devices from different manufacturers and research laboratories.

1.5.3 Characterization of a solar cell

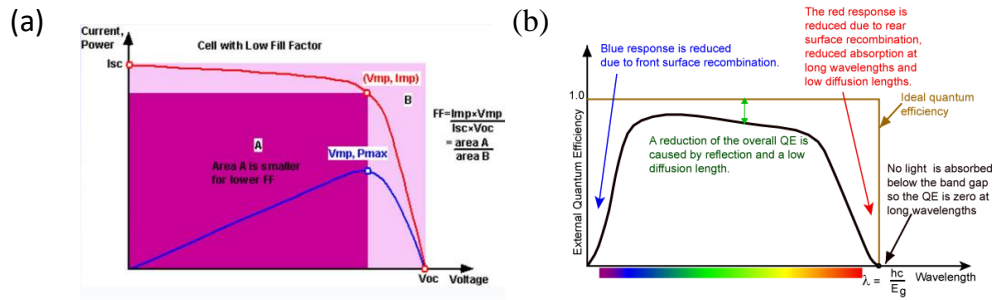


Figure 6: (a) J-V curve and MPP Point, (b) EQE curve from PVEducation

The basic parameters used to evaluate the performance of PVs are as follows⁵²:

- Short Circuit Current (I_{sc}): It is the current in the circuit when the load is zero in the circuit ($V = 0$).
- Open Circuit Voltage (V_{oc}): is the maximum voltage available from a solar cell, this occurs at zero current. V_{oc} corresponds to the amount of forward bias on the solar cell due to the electric field formed from light generated current.
- Maximum Power Point (MPP): the point on the I-V curve where the highest value of voltage and current correspond, or the highest maximum power output.
- Fill Factor (FF): This is the ratio of the maximum power point to the product of open circuit voltage (V_{oc}) and the short circuit current (I_{sc}). Graphically, the FF is a measure of the “squareness” of the solar cell and is also the area of the largest rectangle which will fit in the IV curve:

$$FF = \frac{P_{max}}{V_{oc} \times I_{sc}} = \frac{I_{max} \times V_{max}}{V_{oc} \times I_{sc}} \quad (5)$$

- External Quantum Efficiency (EQE): defined as the number of generated electrons per incident photon, without correction for reflection losses. Under monochromatic light illumination at a wavelength λ (nm) the EQE is defined by equation:

$$EQE = \frac{I_{sc}}{P_{in}\lambda} \frac{hc}{e} = \frac{1240 I_{sc}}{P_{in}\lambda} \quad (6)$$

Where h is the Planck's constant (J s) and c is velocity of light (m s⁻¹).

- Power Conversion Efficiency (PCE): ratio of the energy output from a solar cell to input energy from the sun. PCE depends on the solar spectrum and intensity of the incident sunlight and the temperature of the solar cell. The efficiency, η , of a solar cell is determined as a fraction of incident power which is converted into electricity and is defined as:

$$P_{max} = V_{OC} I_{SC} FF \quad (7)$$

$$\eta = \frac{V_{OC} I_{SC} FF}{P_{in}} \quad (8)$$

The input power for efficiency calculations is 1 kW/m² or 100 mW/cm².

1.6 Solar cell principles

1.6.1 Semiconductors and p-n junctions

Homo-junctions (a junction between n- and p- type layers of the same semiconductor material), hetero-junction (junctions between two different semiconductor materials both include intervening with an insulating layer. Homo-junction solar cells have been studied in great detail because of their application in rectifiers and transistors, hetero-junction solar cells are used mostly in solid state lasers and light emitting diodes^{53, 54}. An overview of the current transport through a junction device is described below.

1.6.1.1 .Homo-junction solar cells

A homo-junction is formed when a p-type and n-type semiconductors of the same material come in contact with each other; a potential is formed. The Figure 7 (left) shows the band diagram of p and n-type semiconductors at equilibrium. The n-type region has a high concentration of electrons while the p-type region has a high concentration of holes. The Fermi energy level is the maximum energy of an electron at 0K which is closer to the valence band (VB) in the p-type semiconductor and is closer to the conduction band (CB) in the n-type semiconductor^{55, 56}. When the p and n-type regions come in contact, the majority carriers from the n-region (electrons) diffuse into the p-region. Similarly, the majority carriers from the p-region (holes) diffuse towards into the n-region. This diffusion of charge carriers constitutes the diffusion current and leaves behind uncompensated charge of acceptor ions (negative) and donor ions (positive) respectively. The uncompensated charge creates an electric field, which is called the built-in electric field⁵⁵. This electric field is spread across a region called the depletion region (also called the space charge region) and creates a drift current which is equal and opposite of the diffusion current. The potential caused due to the accumulation of uncompensated charges on either side of the junction is called built-in potential, V_{bi} .

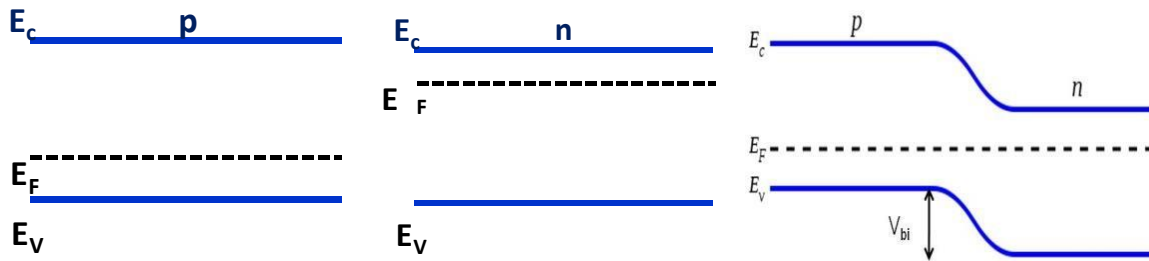


Figure 7: p- and n-type semiconductors before contact (left & center), p-n junction at equilibrium (right)

Under thermal equilibrium, the Fermi energy is spatially continuous across the p-n junction. As a result, the conduction and valence bands bend by an amount equal to qV_{bi} . This is called the potential barrier and it represents the energy an electron on the n-side has to overcome to go over to the conduction band on the p-side⁴⁹. The band diagram of a p-n junction under equilibrium is shown in Figure 7 (right).

The built in potential is given by:

$$V_{bi} = \left(\frac{kt}{q}\right) \ln \left(\frac{N_A N_D}{n_i^2}\right) \quad (9)$$

Where, N_A and N_D are acceptor and donor concentrations in the p and n-type regions, n_i is the intrinsic carrier concentration. K is the Boltzmann constant, and T is the absolute temperature.

When a p-n homo-junction is forward biased, the majority of the applied voltage (V_A) drops across the depletion region^{55, 57}. Therefore, the potential barrier decreases by an amount equal to the applied voltage. The electrons on the n-side can now readily overcome the barrier to reach the p-side. The band diagram of a p-n junction under forward bias is shown in Figure 7 (left).

Under reverse bias, the applied voltage adds to the built-in potential and the electrons on the n-type region have a higher barrier to crossover to the conduction band of the p-type region⁵⁸. The barrier is now given by the following equation:

$$V_{bi} = (q) \times (V_{bi} + V_a) \quad (10)$$

The current-voltage relationship of a p-n junction in equilibrium is given by Eq. (2.10)

$$I = I_0 \times (e^{\frac{qV}{AKT}} - 1) \quad (11)$$

Where, I_0 is the reverse saturation current, A is the diode quality factor which always lies between 1 and 2 describing the dominant recombination in the junction.

1.6.1.2 Hetero-junction solar cell

Heterojunctions are formed between two different semiconductor materials. When a junction is formed, as in the case of homo-junctions, the Fermi energy is constant throughout the material under equilibrium conditions⁵⁹. The major difference between a homojunction and a heterojunction is the barrier height seen by the carriers (electrons and holes)⁶⁰. In the case of a homojunction under equilibrium, the barrier height seen by the electrons and holes was equal to the built-in potential V_{bi} . Therefore the magnitude of hole and electron currents is determined by the doping levels⁵³. In the case of a heterojunction, the barrier is not the same as seen by the electrons and holes due to a difference in the built-in potentials on the n- and p- sides. The barrier height for electrons is larger than for holes.

1.6.2 Solar cell operation

A photovoltaic system uses the absorber layer to capture the sunlight (photons). If the incoming photon has an energy greater than the bandgap of the semiconductor material, that energy will excite the electrons/hole from the valence -to conduction band (electron) or the conduction- to valence band (hole) and will generate an electron-hole pair that participates in conduction. These carriers are photo-generated carriers and the process is called light absorption. In a p-n heterojunction, the p-type (majority carrier hole) and n-type (majority carrier electron) materials are of two different semiconductors. This leads to the formation of valance and conduction band offsets (gaps) and in doped (impurity, defect) semiconductors, extra energy gaps are added which essentially increases the conductivity with respect to the Fermi level. A CdTe solar cell is sandwiched between n-type CdS and p-type CdTe. The carriers generated close to this depletion region become influenced by the built-in potential, V_{bi} , and become separated by this field. Finally, the separation carriers are collected by metal

contacts at the two ends of the junction. The photovoltaic effect allows for electricity to be generated by using incident photons from the sun to excite electrons to hop across the junction between the energy gap of CdS and CdTe. An electron-hole pair is produced and carriers are transported to their appropriate electrode to participate in conduction.

In heterojunction solar cells with a wide bandgap n-type semiconducting (CdS) and a narrow bandgap p-type semiconductor (CdTe), the wide bandgap semiconductor CdS is called the window layer and the narrow bandgap semiconductor is called the absorber. Photons with energy less than the bandgap energy of CdS will pass through the n-type CdS layer and only photons with energy greater than that of the bandgap energy of CdS will be absorbed. Carriers are generated within a diffusion length of the junction that is collected.

1.6.3 Carrier generation

When light shines on a solar cell, photons with energy greater than the band gap can generate an electron-hole pairs inside the solar cell. Ideally, all the incident photons is expected to be absorbed in the absorber layer. However, this does not always occur, sometimes part of the light is reflected from the front surface before entering the absorber layer, this mechanism is responsible for optical losses. The photon flux density Φ (# of photons/cm² · s) with a single-wavelength (λ) decays exponentially with the depth z ,

$$\phi(z, \lambda) = \phi(z_0) \cdot (1 - R) \cdot \exp(-\alpha\chi(\lambda) \cdot (z - z_0)) \quad (12)$$

Where $\phi(z_0)$ is the photon flux density at the depth of z_0 and $\alpha\chi(\lambda)$ is the absorption coefficient for each layer. The generation rate is given as⁶¹:

$$G(z, \lambda) = -\frac{d\phi}{dz} = \phi(z_0) \cdot (1 - R) \cdot \alpha\chi \cdot \exp(\alpha\chi(\lambda) \cdot (z - z_0)) \quad (13)$$

Equation 21 describes the photo-excited carrier generation rate due to a monochromatic light source. In practice, a spectrum of light shines into a PV solar cell device and usually assumes a one spun spectrum.

1.6.4 Carrier recombination

Ideally, one can assume that all the photo-generated carriers can pass across the junction and be collected by the electron and hole contacts respectively before any loss association with recombination. However, under non-equilibrium conditions, when a semiconductor is taken out of thermal equilibrium by the illumination and/or injection of current, the concentrations of electrons (n) and holes (p) tend to relax back toward their equilibrium values through the process of *recombination*^{62, 63}. Recombination happens when electrons fall from the conduction band back down to the valence band eliminating the valence-band hole. There are several recombination mechanisms that are important to the operation of solar cells- recombination through traps (defects) in the forbidden gap (Shockley-Read-Hall or SRH recombination), radiative (band-to-band) recombination, and Auger recombination.

The *Shockley-Read-Hall* (SRH) recombination does not occur in perfectly pure, non-defected material⁶⁴. SRH is a two-step process, involving: 1.) an electron (or hole) is trapped by an energy state in the forbidden region which is introduced through defects in the crystal lattice. These defects can either be unintentionally introduced or added to the material as in doping, and 2.) If the hole (or an electron) moves up to the same energy state before the electron is thermally re-emitted into the conduction band then it will recombine. The rate at which the carrier moves into the energy level in the forbidden gap depends on the distance of the introduced energy level from either of the band edges⁶⁴. If any energy is introduced close to either band edge, recombination will less likely happen as the electron is likely to re-emit to the conduction band

edge rather than recombine with a hole which moves into the same energy state from the valence band.

Radiative (band-to-band) recombination is the recombination mechanism that dominates in direct bandgap semiconductors⁶⁵. The key characteristics of radiative recombination are⁶⁶: 1.) in radiative recombination, an electron from the conduction band directly combines with a hole in the valence band and releases a photon; and 2.) the emitted photon has an energy similar to the band gap and is therefore only weakly absorbed such that it can exit the piece of semiconductor.

Auger recombination involves three carriers. An electron and a hole recombine, but rather than emitting the energy as a photon, the energy is given to a third carrier, and electron in the conduction band. This third electron then thermalizes back down to the conduction band edge. Auger is most important at high carrier concentrations caused by heavy doping. Auger recombination limits the lifetime and efficiency of solar cell devices.

1.7 Objective of this research

The objective of this research is to improve the overall CdTe thin film solar cell power conversion efficiency through doping engineering to increase the photovoltage and photocurrent properties. The candidates of dopants include Group I (e.g. Copper (Cu) and Silver (Ag)), and Group V (e.g. Arsenic (As) and Antimony (Sb)) for improvement of photovoltage (V_{OC}) which is essential in the improvement of the power conversion efficiency.

The hypothesis for this project:

- To improve the CdTe power conversion efficiency, one way is to improve the carrier concentration and the other way is to improve the carrier lifetime.

- Cu^+ and Ag^+ could substitute the Cd^{2+} site and contribute to additional hole as an acceptor to increase the carrier concentration.
- As^{3-} and Sb^{3-} could occupy the Te^{2-} site and could provide more holes as an acceptor to increase the carrier concentration.

This proposal will also aim to:

- Study the effect of Group I and V dopant defects in CdTe to optimize desired photovoltage properties;
- Dope the absorber layer in CdTe with Group I and Group V elements by solution process methods with cost-effective and suitable for traditional production process;

CHAPTER 2

DOPING ENGINEERING IN CdTe THIN FILM SOLAR CELLS

2.1 Semiconductors

Semiconductors possess conductivities that lie between those of metal and insulators. In their most pure form, these are considered intrinsic semiconductors with low electrical conductivities. Adding dopants to the semiconductor will allow for alternative electronic states within the bandgap that can further assist carriers in participating in conduction and ultimately; increase its conductivity. These type of semiconductors are called extrinsic semiconductors. The process of doping with impurities is called doping with *dopants*. As with any semiconductor, the carrier concentration can be increased by doping the device with specific material to achieve higher p/n-type carrier concentration in CdTe. This work is focused on p-type doping of CdTe. The main factors that limit p-type doping in CdTe are⁶⁷:

1. Low dopant Solubility
2. High dopant ionization energies
3. Formation of oppositely charged defect states which compensate p-doping

CdTe has an ideal bandgap (1.45eV) for optical absorption. Native defects in CdTe influence the acceptor (p-type) carrier concentration, absorption of photons and the lifetime of these carriers which all consecutively alter the V_{oc} . Successful doping leads to higher conversion efficiencies. Knowledge and understanding of defect properties and the difficulty in doping is necessary to

identify the dominating factors that limit the V_{OC} which is a direct association to low doping concentrations and carrier lifetimes in CdTe.

2.2 Defects in semiconductors

A perfect crystal is an ideal situation, it is almost impossible to grow a perfect crystal of any sort. There always will be imperfections in crystals such as voids, impurities or even dislocations at almost all times, regardless of how much effort is put into trying to purify a material. Real materials do not follow a perfect crystalline atomic pattern, they have a polycrystalline structure filled with grain boundaries and impurities that could affect carrier transport in semiconductor devices. Solids prefer their structure to be at its minimum energy. Since every atom in a crystal belongs to a specific lattice site that satisfies its lowest energy state, when defects are introduced, an imperfect crystal structure is energetically preferred because atoms become bound to imperfections making it more difficult to move and results in material strengthening⁶³. Imperfect crystals allow scientist the ability to tailor material properties into a devices. Defects that form electronic states within the bandgap of the material are responsible for the electrical and optical properties of semiconductors. A strong understanding of defects is essential in order to maximize the V_{OC} and other properties in device performance. There is a large variety of possible defects. The simplest way to classify them is through categories according to their dimensionality: point defects, line defects, area and volume defects. In this work, all studies are focused on point defects. These defects can be subdivided into two groups: native and impurity-related defects.

2.2.1 Native (intrinsic) defects

Native defects are classified as point, line, plane or volume defects. A native defect forms when an atom is missing from a position that should to be filled in the crystal which

creates a vacancy⁶⁸. Common defects are vacancies, interstitials and substitutional defects. An interstitial defect forms when an atom occupies an unintended interstitial site⁶⁸. A substitutional defect is formed when atoms of different type exchange lattice positions in a crystal.

Table 1. List of native point defects that can form in CdTe

Notation	Defect Name	Description
V_{Cd}	Cadmium vacancy	Missing Cd atom
Te_i	Tellurium interstitial	Extra Te atom in the lattice
Te_{Cd}	Te at cadmium antisite	Te occupying a Cd site
Cd_{Te}	Cd at Te antisite	Cd occupying a Te site
V_{Te}	Tellurium vacancy	Miss Te atom
Cd_i	Cadmium interstitial	Extra Cd atom in the lattice

2.2.2 Impurity defect

Extrinsic defects arise when dopants (impurities) are intentionally added to a material that occupy lattice sites in an effort to engineer its electronic properties. When impurities are intentionally introduced into the semiconductor they are called *dopants*. Extrinsic point defects affects almost all engineering properties but they are particularly important in semiconducting crystals where extrinsic defects are used to control the electrical properties and increase mechanical strengths of the material⁶³. Impurity defects are added to semiconductors to control the type and concentration of charge carriers.

2.2.3 Trapping problem

Doping concentrations in semiconductors are typically around 10^{-6} ppm⁶⁹, adding impurities to the semiconductor can cause orders of magnitude in increased conductivity. Impurities of the right kind can form energy states close to the conduction band and valence band with ionization energies of a few tens of meV. Because of the presence of grain boundaries, defect states such as shallow and deep states located in the bandgap can modify the conductivity. When defects are introduced, there exist allowed energy states somewhere throughout the

bandgap. Trapped states with ionization or activation energy level less than 0.05 eV from the band edge are (shallow) dopants, and those with greater than 0.05 eV are deep levels⁷⁰. Shallow states are located close to the band edges and can act as sources for electrons and holes, common examples are dopants. Shallow traps are generally created by substitutional doping and it is able to bind an electron (if created by a donor atom) or a hole (if created by an acceptor atom). Deep states are located close to the center of the bandgap, see Figure 8 for examples of both.

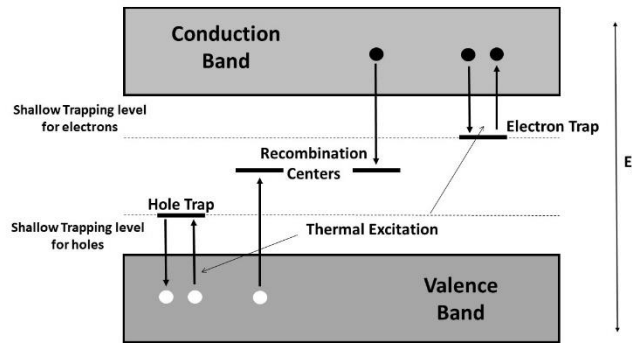


Figure 8: Semiconductor trapping; shallow and deep traps

Deep states can act as recombination centers that hinder charge carriers and reduce the conductivity or result in low doping efficiencies. The deep levels may compensate the dopants, and are mostly treated as traps which are also called Shockley-Read-Hall (SRH) generation-recombination centers that have a negative impact on the performance of most devices. Deep trapping levels in the bandgap can either help or hinder device performance, depending on the energy level associated with the trap and the device. These traps can shorten carrier lifetime in applications which can be a good aspect for fast switches or it could be very bad for solar devices. Some defects can also create their own energy levels in the bandgap of semiconductors leading to the formation of trapping centers for charge carriers. When the charge carriers get stuck on such centers, they either loose time before reaching the edge of semiconductor volume, or vanish due to recombination, shown in the center of Figure 8. Thus, trapping causes

incomplete charge collection in a detector. As mentioned in the previous chapter the energy of the registered particle is proportional to the number of created charge carriers and reflects in the corresponding channel of the multichannel analyzer. This means that if some charge carriers are lost on the way to the anode or cathode, the current pulse registered in the preamplifier will be proportionally smaller and energy data will be sent to a channel of lower energy⁷¹. Nowadays crystal growth technique cannot grow high quality compound semiconductor crystals. Film growth techniques can introduce defects in the material. Some films grown by conventional vapor deposition or solution growth techniques are make it more difficult to dope a certain material because of the presence of interstitials and vacancies. Semiconductors such as CdTe and especially CdZnTe have a high defect density in comparison with high-purity Si or Ge⁷²

2.3 Defects in CdTe

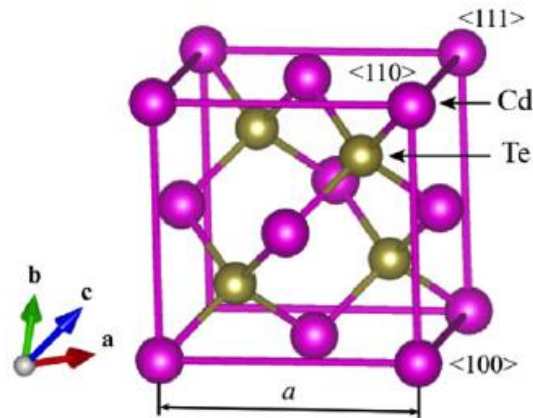


Figure 9: Unit cell of CdTe⁷³

CdTe is the zinc blende structure with a face centered cubic and hexagonal lattice configuration. Each Cd atom is surrounded by 4 Te atoms and vice versa shown in Figure 9. When these atoms become disordered, many defects form which allows the alteration of electronic properties. A description of all native defects in CdTe is given in Table 1.

2.3.1 Role of native point defects in CdTe

Most researchers agree that the principal acceptor defect in p-type CdTe is the cadmium vacancy. However, research holds a major debate on the transition energy of V_{cd} , which ranges from 0.1eV to 0.8eV above the VBM and it is assumed to be found a shallow acceptor defect^{68, 74}. Another native defect is the tellurium vacancy (V_{Te}), which is considered to be a shallow donor defect according to HSE calculations^{75, 76}. This means that V_{cd} has lower ionization energies and can be easily accept holes than other acceptor defects like Te_i . The mechanism between these two defects limit the p-type dopability in intrinsic CdTe. Other donor defects such as, Te_{cd} and Cd_i , also play a key role. The formation energy of these intrinsic point defect levels is a function of deposition stoichiometry and the Fermi energy (E_F). Te-rich deposition is a favorable condition for p-type CdTe, but intrinsic p-type dopability is limited by compensating defects. The maximum achievable hole (acceptor) density is $1.77 \times 10^{14} \text{cm}^{-3}$ with a Fermi level of 0.35eV above the VBM⁷⁵. In order to increase voltage, the hole density and minority carrier lifetime must be increased by two orders of magnitude to the range of 10^{16} - 10^{17}cm^{-3} and $\sim 50\text{ns}$ or higher⁷⁷. Thus doping in semiconductors have two functions: 1. To increase the conductivity by intentionally increasing electron/hole concentration. The conductivity can be precisely tuned by controlling the type and amount of dopants 2. The majority carrier concentration is a constant and temperature independent (near room temperature) so that small variations in temperature will not change the conductivity.

2.3.2 Intrinsic defects

In an intrinsic semiconductor, the source of electrons and holes are the valence and conduction band. The carrier concentration depends exponentially on the bandgap, E_g ⁷⁸.

2.4 Conductivity of a semiconductor

The conductivity of a semiconductor is given by:

$$\sigma = q(\mu_n n + \mu_p p) \quad (14)$$

Where μ_n and μ_p refer to the motilities of the electrons and holes, while n and p refer to the density of electrons and holes, respectively. In a doped semiconductor, where majority carriers greatly outnumber minority carriers, Equation 26 can be reduced to a single term (Equation 27) that only involves the majority carrier.

$$\sigma = pq\mu_p \quad (15)$$

2.5 Temperature dependence

2.5.1 Temperature dependence and doping on mobility

Conductivity of a material is determined by two factors: the concentration of free carriers available to conduct current and their mobility (freedom to move). In a semiconductor, both the mobility and carrier concentration are temperature dependent. Thus, it is important to view the conductivity as a function of temperature which is expressed by

$$\sigma = q[\mu_n(T) n(T) + \mu_p(T)p(T)] \quad (16)$$

There are two basic types of scattering mechanisms that influence the mobility of electrons and holes: lattice scattering and impurity scattering. We have already discussed lattice scattering in the context of metals; we know that lattice vibrations cause the mobility to decrease with increasing temperature. However, the mobility of the carriers in semiconductors is also influenced by the presence of charged impurities. Impurity scattering is caused by crystal defects such as ionized impurities. At lower temperatures, carriers move more slowly so that there is more time for them to interact with charged impurities. As a result, the temperature decreases, impurity scattering increases and the mobility decreases. This is the opposite of the effect of lattice

scattering. The total mobility is the sum of the lattice-scattering mobility and the impurity scattering mobility⁷⁹.

2.5.2 Temperature dependence on carrier concentration

Carrier concentration in a semiconductor is affected by temperature. The intrinsic carrier concentration is given by:

$$n_i(T) = 2 \left[\frac{2\pi kT}{h^2} \right]^{\frac{3}{2}} (m_n m_p)^{\frac{3}{2}} \exp\left[\frac{-E_g}{2kT}\right] \quad (17)$$

Where the exponential temperature dependence dominates $n_i(T)$. To determine the total carrier concentration, we must consider space charge neutrality:

$$n(T) = N_D^+(T) - N_A^- + \frac{n_i^2(T)}{n(T)} \quad \text{and} \quad p(T) = N_A^+(T) - N_D^- + \frac{n_i^2(T)}{p(T)} \quad (18)$$

For doped semiconductors, the temperature dependence of electron concentration is linear. At low temperatures (around $1/T$), negligible intrinsic electron-hole pairs exist (n_i is very small), the donor electrons are bond to the donor atoms. This is the mechanism behind ionization. As the temperature rises, increased ionization occurs and at about 100K all of the donor atoms are ionized. At this point the carrier concentration is determined by doping. The region where every available dopant has been ionized is called the extrinsic (or saturation) region. In this region, an increase temperature produces no increase in carrier concentration.

2.5.3 Temperature dependence on conductivity of a semiconductor

Equation 26 shows that the conductivity depends on both the carrier concentration and the mobility. This means that there are a variety of temperature dependences for conductivity. For example, at low temperatures (less than 200K) the dominant scattering mechanism might be impurity scattering while the carrier concentration is determined by extrinsic doping ($n = N_D^+$), therefore, the conductivity would be seen to increase with temperature. Doping and temperature, depending on the material, will show different temperature dependences of conductivity. An

interesting case happens at high temperatures (above 400K) when the carrier concentration is intrinsic (Equation 30) and the mobility is dominated by lattice scattering ($\mu \propto T^{-3/2}$). In this case, the conductivity is shown as:

$$\alpha \propto \exp\left(\frac{E_g}{2kT}\right) \quad (19)$$

Conductivity then depends only on the semiconductor bandgap and the temperature. In this temperature range, measured conductivity data can be used to determine the semiconductor bandgap energy, E_g .

2.6 Strategies to improve V_{oc}

Most researchers agree that the principal acceptor defect in p-type CdTe is the cadmium vacancy. However, research holds a major debate on the transition energy of V_{cd} , which ranges from 0.1eV to 0.8eV above the VBM and it is assumed to be found a shallow acceptor defect⁷⁴.⁷⁶. Another native defect is the tellurium vacancy (V_{Te}), which is considered to be a shallow donor defect according to outside calculations^{75, 76}. This means that V_{cd} has lower ionization energies and can be easily accept holes than other acceptor defects like Te_i . The mechanism between these two defects limit the p-type dopability in intrinsic CdTe. Other donor defects such as, Te_{cd} and Cd_i , also play a key role. The formation energy of these intrinsic point defect levels is a function of deposition stoichiometry and the Fermi energy (E_F).

2.7 Solution-based doping

Solution-based doping is a cost effective method that has the ability to fabricate large scale cells for simple manufacturing that can easily be integrated into commercial modules. Spin-coating allows for large scale device fabrications at low temperatures which reduce costs associated with the fabrication of solar devices.

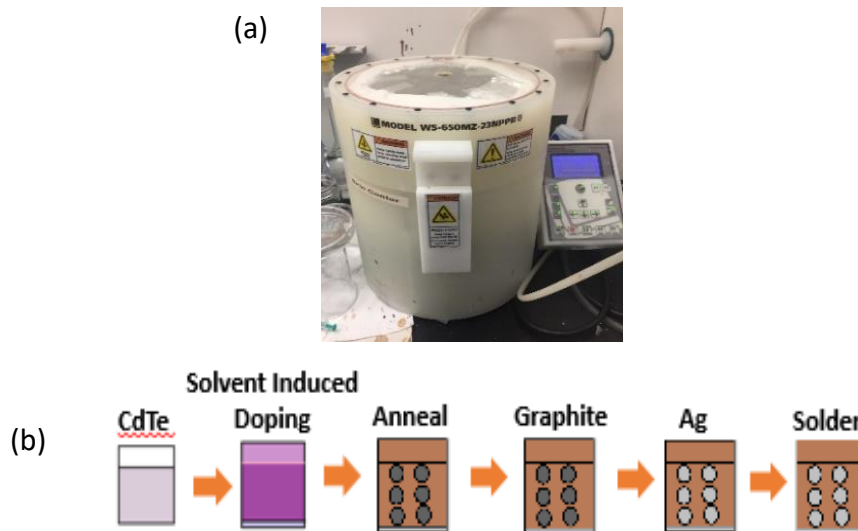


Figure 10: a) Spin-Coater used during the fabrication b) Solution process fabrication method

In addition to being low cost, solution-based solar cell technologies can produce a high throughput fabrication process. In comparison to other in-situ methods that are associated with high system cost and labor cost, this ex-situ method is simple and cost effective. Ex-situ methods could also become an issue when new products cannot be easily integrated into an already established value chain, which could bring hindrance to the production line. Solution based methods provide a fast deposition process with the ability to deposit large deposition areas with high uniformity. In addition, this method could be easily replicated and broadly applied in both the academia and industry settings. Solution processing allows for the deposition of materials by methods such as screen printing, inkjet printing, and spraying which are not only cheap but also with high throughput. The future of solar cells manufacturing processes rely on solution based processing steps for efficiency gains in solar cell devices.

CHAPTER 3

CdTe THIN FILM SOLAR CELL AND EXPERIMENTAL METHODOLOGY

3.1 CdTe thin film PV

PV technology depends on the bandgap of the absorber material used as well as how much light can be absorbed into this absorber material. As stated above, CdTe is a direct bandgap material of 1.45 eV which is responsible for maximal PV conversion into DC current. CdTe also has an optical absorption coefficient (10^4 - 10^5 cm⁻¹) in the wavelength region of 300-1000 nm^{39, 51}. Lastly, CdTe has the ability to form both p and n-type materials which is not seen in many technologies^{38, 39, 80}. Traditional silicon solar cells have a low absorption coefficient because it is an indirect bandgap material, a thick absorber layer for traditional Si solar cells is necessary to maximize the absorption of incident photons from the sunlight. Traditional silicon seems to be a natural choice for PV applications due to cost. Again, this demonstrates why cost is so important in the fabrication of CdTe. In addition, using the relationship $E = hc/\lambda$, (where E is the energy, h is the plank's constant, c is the velocity of light and λ is the wavelength) a material with a bandgap of 1.45 eV calculates to an absorption edge of 850 nm. This means that CdTe can absorb light with wavelengths below 850 nm⁸¹. CdTe has the capability to absorb light throughout the visible spectrum (400 to 900 nm) which furthermore makes this technology so appealing in the industry. Single crystal CdTe devices are practically not ideal simply due to very high surface recombination⁸². Therefore, CdTe is typically used in conjunction with CdS, which acts as an n-type window layer responsible in forming a junction with CdTe to admit maximum amount of light to the junction. We typically chose a window layer with, 1.) A wide

bandgap, 2.) Minimum lattice mismatch of crystal structure, 3.) Virtually no band offset, 4.) Capable of holding larger doping densities. A successful window layer should maximize the transport of carriers with minimum recombination losses while also assisting in forming a junction with the absorber layer to maximize carrier transport to the back contact.

3.2 CdTe current status

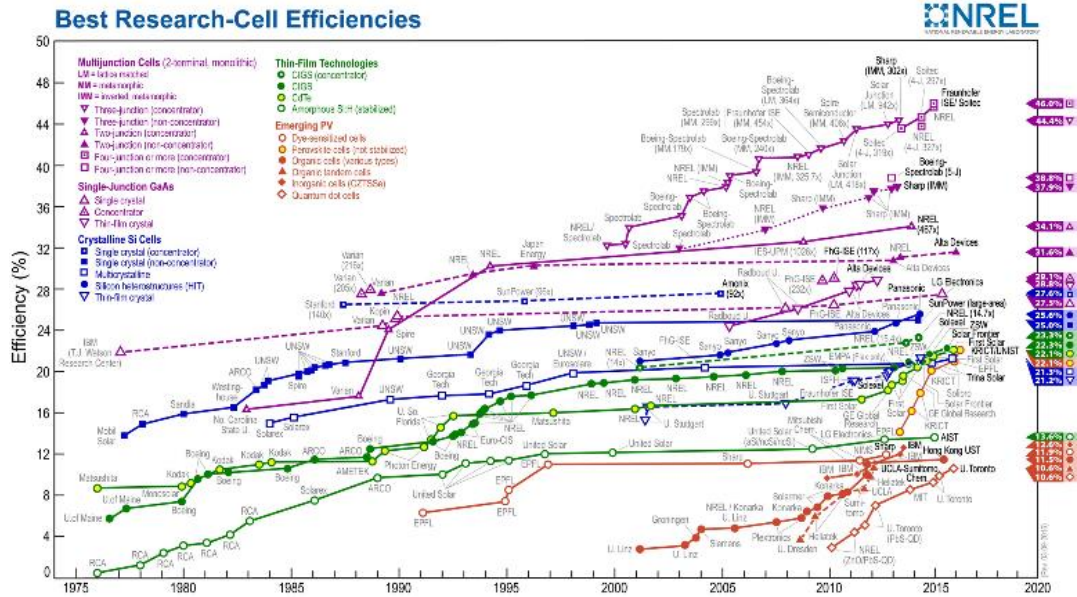


Figure 11: Solar cell efficiency roadmap²⁹

In recent years, different methods of photovoltaics technologies have attracted significant interest due to their high power conversion efficiency, cost effective fabrication, large scale manufacturing and added functionality such as flexibility, being aesthetic and light weight capabilities. Currently, the highest efficiency commercial panels are about 16.5% efficient and most efficient lab cells have reached an efficiency of about 22.1%²⁷. The best V_{OC} for CdTe thin films is 0.87V with a J_{SC} of 30.25mA/cm² and a FF of 79.4%²⁹. The limits predicted by the Shockley-Quisser theory suggest an V_{OC} of ~1.2V, a J_{SC} density of ~31mA/cm², and a FF of 90%, respectively³⁸. The record J_{SC} density in CdTe research has approached its theoretical limit with the FF coming in at desirable high levels. However, after many optimized group studies the

V_{OC} has remained unchanged at 840-880mV which is far below the theoretical limit⁸³. This research intends to address the low V_{OC} limits established using dry and in situ fabrication methods.

3.3 Environmental concerns for CdTe

Vocal opposition has emerged from CdTe modules due to the concern of potential emissions of cadmium from the device. Elemental cadmium, the parent compound of CdTe, is a highly toxic lung carcinogen which is known to cause cancers and targets the body's cardiovascular, renal, gastrointestinal, neurological, reproductive and respiratory systems. Fortunately, CdTe is more stable and less soluble⁸⁴. Manufacturing CdTe solar cells can cause occupational health risks because cadmium compounds are used in powder and liquid forms that can be accidentally dispersed⁸⁵. However, the US photovoltaic industry is vigilant in preventing health risks, and has established proactive programs in industrial hygiene and environmental control^{85, 86}. In addition, toxic compounds must enter the human body through inhaling and ingesting to become harmful. The only pathways by which people might be exposed to PV compounds from a finished module are by accidentally ingesting flakes or dust particles, or inhaling dust and fumes⁸⁴.

3.4 PV Solar cell technology

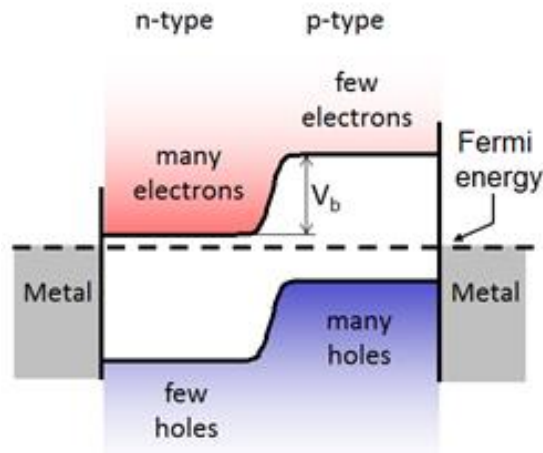


Figure 12: p-n junction at $T=0K$ ⁵² (PVEDUCATION)

3.5 Solar cell device structure

A photovoltaic system uses the absorber layer to capture the sunlight (photons). If the incoming photon has enough energy, this energy will excite the electrons/hole from the valence - to conduction band (electron) or the conduction- to valence band (hole) which will ultimately participate in conduction⁸⁷. In a p-n heterojunction, the p-type (majority carrier hole) and n-type (majority carrier electron) materials are of two different semiconductors. This leads to the formation of valance and conduction band offsets (gaps) and in doped (impurity, defect) semiconductors, extra energy gaps are added which essentially increases the conductivity with respect to the Fermi level (E_F)⁸⁷. For example, a CdTe solar cell is sandwiched between n-type CdS and p-type CdTe. The photovoltaic affect allows for electricity to be generated by using incident photons from the sun to excite electrons to hop across the junction between the energy gap of CdS and CdTe⁸⁸. An electron-hole pair is produced and carriers are transported to their appropriate electrode to participate in conduction. Successful large scale commercialization of solar energy depends on three criteria: efficiency, lifetime and cost.

3.6 CdTe solar cell technology

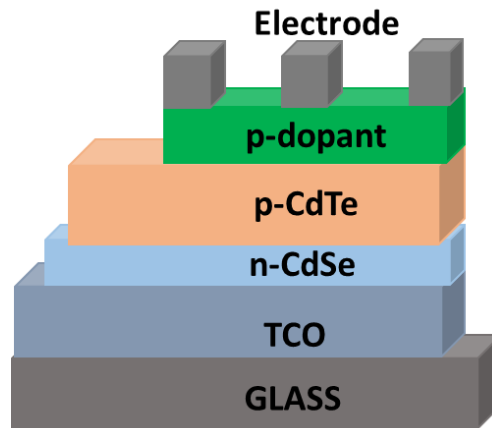


Figure 13: CdSe/CdTe Device Structure

The CdTe solar cell is one of the most promising thin film PV technologies ever studied. CdTe has a nearly ideal band gap of ~ 1.45 eV to convert sunlight into electricity and is a direct band gap material. CdTe has an absorption coefficient greater than $5 \times 10^5 \text{ cm}^{-1}$ in the visible range allowing for 99% absorption of photons with up to 855nm wavelengths⁷⁴. Furthermore, in a heterojunction CdS/CdTe solar cell, the n-type CdS layer is made very thin (cost-effective) and the electron-hole generation is mostly in the p-type CdTe absorber layer as shown in Figure 13. The electrical conductivity of a semiconductor is controlled by extrinsic doping which alter desired photovoltaic properties leading to increased acceptor density (up to 10^{17} cm^{-3}) and increased minority carrier lifetimes (nanoseconds) as well as free carrier mobility which ultimately improve the power conversion efficiency of the solar cell⁸⁰. Because CdTe is a polycrystalline material, this creates grain boundaries that produce defect states located in the bandgap in which can modify the conductivity.

In addition, a high J_{sc} and FF require good carrier collection. Drift through the junction, diffusion across the junction and the constant absorption coefficient all balance each other for good carrier collection probability^{81, 89}. The junction shrinks with increasing acceptor (doping)

density and the diffusion length increases with lifetime while the optical absorption stays constant⁹⁰. CdTe thin films can be deposited by various low-cost methods, such as close spaced sublimation (CSS), electro deposition, spray deposition, screen-printing, and physical vapor deposition (PVD)^{63, 81, 89, 91-98}. Each layer has different physical and chemical properties which overall affect the performance of the device. Since each layer has different crystal structures, microstructure, lattice constant, work function, thermal expansion coefficients, diffusion coefficient, electron affinity, chemical affinity, carrier mobility, mechanical properties ect... there exists, stress, defects, surface recombination centers, chemical changes that affect the interface of each layer causing electrical and optoelectronic property changes. Care must be taken in selecting materials for these layers and careful fabrication of these layers. Glass is chosen by quality, a good conductivity and transparency is important. The glass is also responsible for providing thermal stability for the high temperature deposition of CdTe and the chemical stability of CdS. The transparent conductive oxide (TCO) chosen must have a high bandgap ($E_g > 4\text{eV}$), high transparency, low sheet resistance, high surface quality and high transmittance. Due to its stronger mechanical and chemical stability at high temperature. Front contact must be able to carry the current of the solar cell and be transparent for the incident light. In order to be transparent for visible light, a bandgap of 3.3eV is required⁹⁹. The choice of TCO depends on the absorption edge of the thin film solar cell, for CdTe and Si absorption edge is below 900nm, fluorine-doped tin oxide FTO or indium tin oxide ITO are also suitable choices. The buffer (window) layer of the device, typically CdS for CdTe is deposited via closed spaced sublimation (CSS) or chemical bath deposition (CBD). This layer's responsibility is to form a junction with the absorber layer while admitting maximum amount of light to the junction. The hole transporting layer (HTL) is responsible for successfully transporting carriers to the back

contact for collection. The back contact (BC) is typically graphite, it must have high carrier mobility, high thermal conductivity, great transparency and high melting point. Low cost and great flexibility is the primary requirements for choosing the right BC. The electrode is responsible for collection.

Due to the lack of photovoltaic research on doping CdTe with a solution-based method, solution-processed doping depositions will be performed to further increase CdTe solar cell photovoltaic properties without dramatically increasing the cost of manufacturing. Because CdTe are two different types of semiconductors, they form a forbidden energy bandgap free of electronic states creating a junction barrier between the two semiconductors. This bandgap is the hallmark that differentiates metals, semiconductor and insulators. When dopants are introduced they add allowed energy states in the bandgap which can provide a pathway electrical charge carriers (electrons or holes) to participate in conduction¹⁰⁰. Shallow states act as dopants that are located close to the band edge near the valence/conduction edge, these states can be easily ionized. Deep states are more difficult to control in which are located deep within the forbidden region close to the center of the bandgap and act as deep traps or charge carriers “killers” that decrease promote recombination and decrease conductivity. Deep states also reduce minority carrier lifetime and some deep states can actually pin the Fermi level near the middle of the energy gap leading to high resistive materials¹⁰⁰. In an intrinsic semiconductor, the Fermi level is located in the middle of the bandgap. The Fermi level is shifted by the type of dopant used, either toward the conduction or the valence band giving information about which carriers are responsible for conduction. Film growth techniques also introduce defects in a material that affect the conductivity. Almost every device processing step that involves wet chemicals will introduce hydrogen which can produce high series resistivity or confine electrical currents to a

specific leading to J_{sc} limitations¹⁰¹. For this reason, careful fabrication will be performed to limit interferences with hydrogen during the solution based processing.

3.7 CdTe challenges

3.7.1 Shockley-queisser-limit (s-q limit)

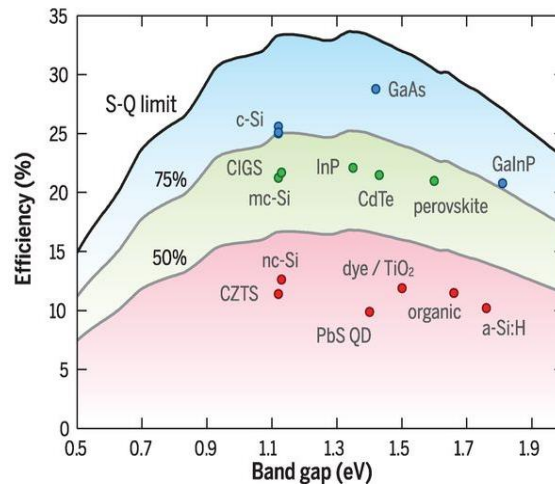


Figure 14: Theoretical efficiency limit for various solar cell technologies⁶⁴

Not all the incoming sunlight can be converted into electricity. The average amount of the sun's radiation that penetrates the atmosphere and reaches the earth is 51% of the total incoming energy (30% is reflected back into space and 19% is absorbed by the atmosphere and clouds)¹⁰². Of this 51% of the radiation that reaches the earth, theoretically calculated by Shockley and Queisser (SQ) for a silicon solar cell, only 33% can be converted to the electricity (S-Q limit). The Shockley-Queisser limit refers to the maximum theoretical efficiency of a solar cell using a single p-n junction. This limit is one of the most fundamental to the solar energy production with photovoltaic cells and is considered to be one of the most important contributions to the phenomena¹⁰³. According to Figure 14, CdTe has the ability to reach solar cell efficiency of 25%¹⁰⁴.

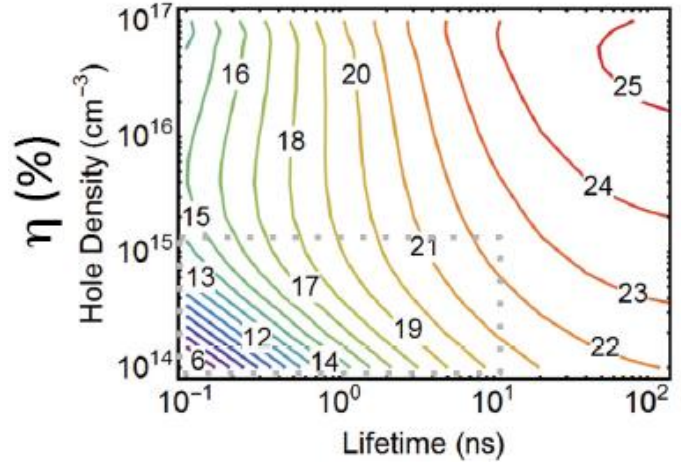


Figure 15: Formation energies of Group I Dopants in CdTe⁹⁰

The limitations in V_{OC} primarily arise from its low p-type (acceptor) density (10^{14} - 10^{15}cm^3) and short minority carrier lifetimes (few nanoseconds). Traditionally, a post-deposition heat treatment, cadmium chloride CdCl_2 heat treatment, is used to improve grain growth and the quality of the grain boundaries during recrystallization where Cl prefer to stay⁹⁶. Crystal growth provides a way of understanding the effects of doping. CdCl_2 is placed on the back contact of the cell and annealed. Moreover, the Cl-treatment is also effective at removing native structural defects and promoting intermixing between CdS and CdTe at their interface³⁹. To achieve an V_{OC} of greater than 1V, the acceptor density and minority carrier lifetime need to be simultaneously increased to the range of 10^{16} - 10^{17}cm^{-3} and $\sim 50\text{ns}$ or higher, respectively^{82, 105}. Therefore, increasing p-type doping and minority carrier lifetime is priority for increasing CdTe device efficiency to and above 32%⁹⁰. Additionally, increased doping causes the junction barrier to decrease, the fermi level will decrease and carrier mobility will play a tremendous role in maintaining high short circuit current (J_{sc}) because of more stringent requirements on the minority carrier diffusion length. A hole concentration of $>10^{17}\text{cm}^{-3}$ and lifetime of $>10\text{ns}$ are expected with efforts to lead the device efficiency of 32% and V_{OC} of more than 1V. The limitations in CdCl_2 post-deposition heat treatment are believed to be caused by compensation

effects in defect chemistry. A chlorine atom is supposed to substitute a tellurium atom and act as a donor. However, when a large number of V_{Cd} are present, the chlorine can form a defect complex with the cadmium vacancy that acts as a shallow acceptor. In order to make CdTe a good p-type semiconductor, the amount of these defect complexes should be significantly higher than the amount of chlorine substituents.

Unfortunately, compensation issues can arise during doping. Acceptor dopant atoms introduce the formation of low energy complex center defects that interfere with doping. These shallow acceptors can provide free holes for conduction to turn into deep-level defects. This conversion to deep centers are termed AX centers that refers to some acceptor A combined with an unknown defect X that form deep level centers or self-compensated acceptor-induced defects that acts as a donor to compensate the acceptor⁸². In addition, if we dope too low, efficiency may suffer as a result from low dopant solubility, high dopant ionization energy, defect compensation, dopant self-compensation, or a combination of the above¹⁰⁶. If doping is too heavy in a semiconductor, it undergoes a metal to insulator transition. This happens when there are so many dopant atoms of the same type that electrons can easily hop from one dopant to another to another, and thus travel long distances through the lattice without changing their energy leading to an insulator transition. It should also be noted that the AX center is not the only source of p-type doping limitations, in some cases, the acceptor level can be deeper than imaged leading to pinning in the Fermi Level which creates an energy barrier for carriers by bending the band at the interface degrading the performance in devices.

Charged particles (shallow and deep defects) have a problem with self-compensation especially when dealing with wide-bandgap semiconductors. Self-compensation happens when charged impurities become compensated not only by a change in electron/hole concentration but

also by a change in vacant defect concentrations. The degree of self-compensation is a function of the host material and the dopant concentration. It is also theoretically proven that donors are compensated mostly by native ionic defects which is shown in p-type semiconductors⁸². Self-compensation is dependent on the nature of the host material and the amount of dopant used. Self-compensation can also be seen as the deviation from unity for both hole/electron concentration where the dominant conductivity may change from p-type to n-type depending on the degree of self-compensation. It can exist in narrow bandgap semiconductors but more pronounced in wider bandgap semiconductor materials. In addition, it has also been theoretically proven that native defects contribute to self-compensation of the dopant but do not lead to Fermi level pinning. Extrinsic dopants however, yield donors and acceptors that, at high concentration, result in pinning of the Fermi level that creates an extra energy barrier which hinders conductivity¹⁰⁷.

3.7.2 How to overcome these barriers

The ability to controllably dope the p-type layers of a solar cell during growth is key to higher performance and simplified manufacturing. Figure 15 shows the efficiency limit that can be obtained for a specific dopant concentration with a precise lifetime. If research can increase the carrier concentration and the lifetime of the carriers through careful architecture and fabrication, a theoretical limit of 32% for CdTe is possible. A hole concentration of $>10^{17} \text{ cm}^{-3}$ and lifetime of $>10\text{ns}$ are expected with efforts to lead the device efficiency of 32% and V_{OC} of more than 1V^{90} . Additionally, if the depletion width is decreased by increasing doping, decreased Fermi level, photocarrier mobility will play a tremendous role in maintaining high short circuit current (J_{sc}) because of more stringent requirements on the minority carrier diffusion length. The ability to controllably dope the p-type layers of a solar cell during growth is key to higher

performance and simplified manufacturing. Other avenues such as incorporating Cu, Ag, As and Sb will be employed to improve the photovoltage.

3.8 Fabrication process

This fabrication process is simple yet an effective way to enhance the ability for minority carrier collection. The fabrication process starts with an initial extensive cleaning step which includes a pre-cleaning step. The pre-cleaning step is a type of “brushing” where a water-detergent solution and water will assist in the removal of organic contaminants, metal particles or other random features that may be on the wafer surface. This process is essential to enhance light absorption.

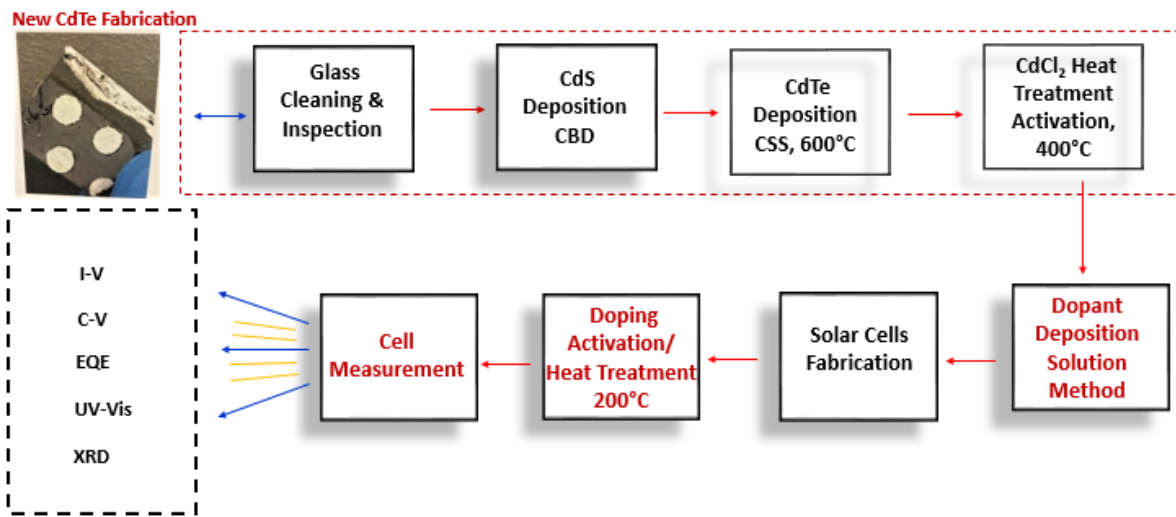


Figure 16: CdTe solar cell fabrication process

The substrates were thoroughly cleaned under running de-ionized (DI) water with DI water followed by a very short 10% HF solution as shown in Figure 16. The deposition of CdS was done by chemical bath deposition (Cds). CBD is an easy process for the fabrication of CdS thin films on ITO glass. The substrate is placed in a hot chemical bath solution while stirring vigorously for a specific amount of time, positive and negative ions will reach and meet on the

substrate and a thin film will grow. The thickness of this layer is typically 60-80nm, dependent on the deposition time and molecular weight of CBD. CBD does not require a vacuum nor high temperatures which makes this process unique and favorable. This process is followed by the high temperature deposition of CdTe performed using the closed-spaced sublimation (CSS) method which will be talked about in more detail shortly. A high temperature deposition of CdTe is required to enhance the inter diffusion at the CdS/CdTe interface to achieve high quality junctions between each layer. In addition, it is necessary to deposit CdTe in a controlled atmosphere in order to control the atoms so they will not re-evaporate from the substrate. CdTe was deposited at a source temperature of 600°C for 10mins. The CdCl₂ was then performed at a temperature of 400°C to promote the inter diffusion at the junction of CdS/CdTe, improve the quality at the grain boundaries and remove native structural defects that may hinder device performance. The dopant deposition solution method was performed in many different steps with different parameters ranging from various deposition rates/times and precursor molecular compositions in an effort to fabricate our best champion cells with the highest device performance. The dopant activation process was performed at 200°C to enhance the activation of carrier concentration and transport to the back contact for collection. A lower temperature was performed here to lower energy consumption and substrate stresses that may hinder carrier transport. Cell measurements were performed on champion cells. XRD and UV-Vis results are not included in this work because the fabrication of CdTe was collaborated for colleagues in Ohio in an effort to reduce the environmental concern associated with environmental, health and safety requirements required for graduate students at the UA. The XRD in this work was used to confirm the crystallinity of the deposited CdTe layer and the UV-Vis was used to measure the

intensity of light passing through the sample which can also be characterized by using the EQE and I-V which has been performed in this work.

3.8.1 Glass substrate and transparent conductive oxide (TCO) layer

Corning Eagle XG, an alkaline earth boro-aluminosilicate glass (alkali-free), was used as the substrate due to its high optical transmittance (up to 90% in the wavelength range 350-2200 nm), mechanical strength and high temperature tolerance. The dimension of the substrates was 1.45" x 1.32" with a thickness of 0.7 mm. The glass is typically the thickest part of the solar device with a thickness of around 3mm. The substrates were thoroughly cleaned under running de-ionized (DI) water with DI water followed by a very short 10% HF solution. This fabrication of CdTe was prepared elsewhere due to the carcinogen nature of elemental cadmium. The glass is an extremely important aspect in device performance. The glass needs to be of high quality adequate glass with good conductivity and transparency to light and haze (ability of a layer to trap light). The glass plays an important role in determine PCE%. The thickness of the glass is important at providing thermal stability for the high temperature deposition of CdTe while also providing chemical stability for CdS.

A bilayer of transparent conductive oxide (TCO) was used as the front contact of the CdTe photovoltaic devices. The TCO layer was deposited by RF sputtering. The TCO was the conductive layer with a thickness of 3000 Å, deposited at 250 °C. The TCO layer has a typical sheet resistance of approx. 2-15 Ω. The front contact must be able to carry the current of the solar cell and be transparent for the incident light. In order to be transparent for visible light, a bandgap of at least 3.3eV is required, TCO has a high bandgap energy of 4eV. It has high transparency, low sheet resistance and high surface quality with low pinholes and low roughness. A transmittance of between 80-90% is typically requires due to its strong mechanical and

chemical stability at high temperature. The choice of TCO depends on the absorption edge of the thin film solar cell, for CdTe and Si absorption edge is below 900nm, fluorine-doped tin oxide FTO or indium tin oxide ITO are also other suitable choices. They are all typically sputter deposited on the glass. The deposition of TCO was done elsewhere and the substrates were thoroughly cleaned under running de-ionized (DI) water with soap, acetone, IPA and DI water repeatedly.

3.8.2 Window layer: cadmium sulfide (CdS)

CdS is a suitable n-type material which could have been fabricated with different techniques including chemical bath deposition (CBD), thermal evaporation, chemical vapor deposition (CVD), molecular beam epitaxy (MBE), traveling heater method (THM), or spray pyrolysis. Each of these deposition techniques provide different optical, structural, electrical and morphological properties all of which have the ability to deposit CdS but vary in cost effective methods. CdS is called the window layer due to its higher rate of light transmission¹⁰⁸. The responsibility of this layer is to form a junction with the absorber layer while admitting maximum amount of light to that junction. This layer is responsible for providing maximum absorption and transport of carriers with minimum recombination and electrical losses. We typically pick a material for this layer with 1.) Wider bandgap 2.) Minimum lattice mismatch of crystal structure 3.) Virtually no band offset 4.) capability of holding larger doping densities¹⁰⁸. CdS is used to decrease the diffusion of atoms from the TCO to the rest of the film, improve the surface morphology of TCO with respect to roughness and pinholes and to ensure the deposition of CdS films with thin thicknesses. Due to the poor electrical properties of CdS, light absorbed in CdS layer does not convert to photocurrent. For this reason, the CdS layer needs to be as thin as possible, while still thick enough to prevent the formation of pinholes. Pinholes are usually

located on the top later of the solar cell. CdS thin films is suitable for other semiconductor devices and radiation detectors. CdS has a wide bandgap and highly used in photovoltaic devices. CdS should be fabricated very thin so a high amount of light can pass through CdS and be absorbed in CdTe. The CdS should be continuous to reduce the changes of short circuiting and the CBD deposition method is used to fulfill this requirement. The thickness of CdS is very important for high efficiency devices. CdS thin films are grown by cadmium chloride, ammonium nitrate, and potassium hydroxide, after heating to a specific temperature, thiourea is added to start the fabrication.

3.8.3 CdTe thin film deposition

The CdTe thin film was deposited using the closed space sublimation by our collaborators. The films characterization and treatment was finished in our own lab. The CdTe film with $\sim 3 \mu\text{m}$ was deposited on the CdSe buffered F doped SnO_2 (FTO, NSG USA) substrate using the close space sublimation (CSS). The CdTe solar cell substrate configuration is shown in Figure 17. The detailed CSS deposition process was reported elsewhere.¹⁰⁹

Closed-Spaced Sublimation is a type of thermal evaporation technique used to deposition thin films for the fabrication of operational devices. The advantage of this techniques is its simplicity and high transport efficiency conducted under low vacuum conditions and moderate temperatures that will reduce energy consumption. In this technique, the source material is placed in a solid powdered form the graphite boat which is heated by the halogen lamps provided in the system.

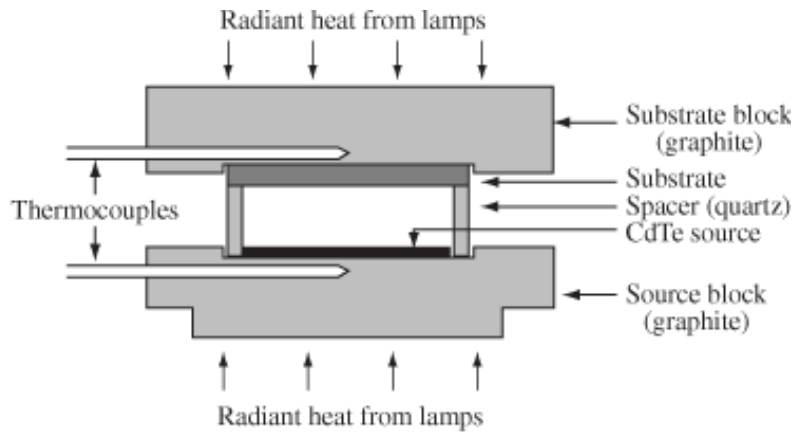


Figure 17: Schematic view of closed-spaced sublimation (CSS) apparatus

The substrate is placed in a sheet that acts as a thermal gradient between the source and the substrate. The source is heated to its melting temperature which the substrate is held at some lower temperature, the material from the source starts to sublime and deposit onto the substrate and a thin film is produced. The CSS is a facility for thin film deposition of materials and it is shown in Figure 18.

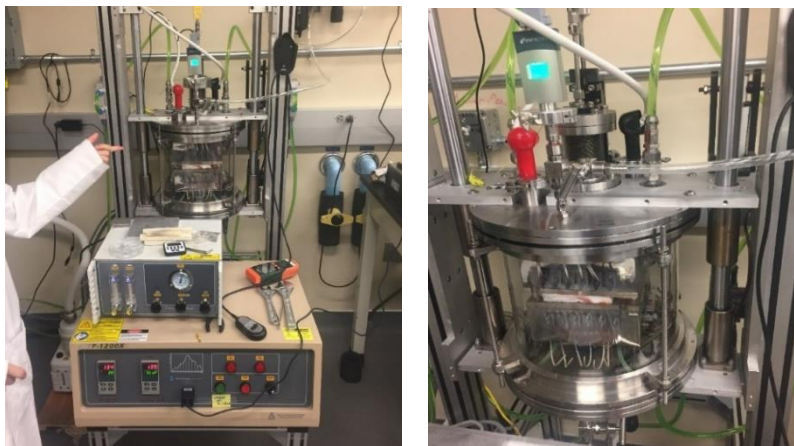


Figure 18: CSS system

Before the fabrication of thin films by CSS, the substrates must first be properly cleaned with acetone, isopropyl alcohol, and rinsed with DI water and an ultrasonic cleaning. The quality of the film, material transport and deposition rate is dependent on the fabrication parameters¹¹⁰.

CdTe is typically deposited at a high temperature to provide good control in the growth and good performance in device. High series resistivity in the device is also reduced by increasing the substrate temperature as well as higher deposition rates has improved at high substrate temperatures¹¹⁰. Annealing is typically done right after the deposition of the absorber layer using CSS to provide improvements in surface morphology and reduce roughness associated with the surface of CdS and CdTe films. Recombination centers that are known to hinder carrier transport has been seen to reduce during the annealing¹¹⁰. The crystallinity of the film also improves during the annealing, an improved V_{oc} has been known to improve after the annealing with further improves device performance¹¹⁰. CSS has a moderate temperature deposition method that produces encouraging results which is mainly because it is simple, has high transport efficiency and the deposition can be done in a low vacuum at moderate temperatures. A well-known disadvantage to CSS is its inability to introduce a thickness monitor.

This layer is so important because the absorption of light and the generation of carriers happens in this layer. The film thickness was in the range of 4-7 μm . CdTe could be deposited many different ways like sputtering, electrodeposition (ED), traveling heater method (THM) and others but because I focused this study on a cost-effective approach, CSS was chosen to reduce energy consumption and cost associated with the fabrication of CdTe. The bandgap of this layer needs to be small enough to allow absorption of an appropriate portion of the solar spectrum while it also has to be large energy to minimize any bias reverse stresses like heat and humidity. There is a disadvantage to choosing CdTe as an absorber layer and this stems from the fact that CdTe has a high resistivity and work function that affects the semiconductors metal union with the back contact. This effect is typically minimized by the CdCl_2 activation treatment to remove native structural defects associated with the deposition of CdTe.

3.8.4 Cadmium chloride (CdCl₂) heat treatment

The CdCl₂ heat treatment (HT) activation method is a well-know, necessary step for high-efficiency CdTe solar cells. This technique is performed on most devices to increase grain size, improve the quality at the grain boundary, remove native structural defects that may hinder carrier transport and promote the intermixing of CdS/CdTe. The optical, structural and morphological changes of CdTe and CdS surfaces on CdTe/CdS/ITO/Glass solar cells due to the activation CdCl₂ treatment solution at 400 °C for 30 mins in ambient air. The temperature and time in this process was chosen due literature reviews and trial and error. The CdCl₂ concentration and the annealing temperature and time were systematically screened. For example, the annealing temperature was from 390 to 420 °C and the CdCl₂ concertation was selected from 10 g/L to 100 g/L. The annealing time was tailored from 20 min to 40 mins. Our champion cells came from cells that were activated at this temperature and once experimentally proven that this parameters worked in the fabrication, these parameters were used throughout the entire study. The CdTe surface was washed using deionized water (DIW) to remove the residual CdCl₂, following an etching process using the diluted HCL solution to remove the surface oxides layer.

This post deposition process heat treatment has been demonstrated in the literature to improve the short circuit current (J_{sc}) and open circuit voltage (V_{oc}) of CdTe/CdS thin film solar cells by recrystallization, reorientation and grain enhancements that ultimately enhance device performance. Heat treatment itself has the ability to enhance the grain size through recrystallization but when combining heat with CdCl₂, the Cl has been seen to accumulate at the grain boundary and remove structural defects while also enhancing the quality of the junction, this process has been known to be a key step in high quality CdTe/CdS solar cell device

performance. There are different methods of CdCl_2 treatments that are used in the industry, solution CdCl_2 treatment, evaporated CdCl_2 treatment and vapor CdCl_2 treatment, all of which have been known to activate the chemical reaction between CdTe and CdS , which is the driving force of the bulk and grain boundary inter diffusion of CdTe and CdS . Regardless of which method used, the basic mechanism by which CdCl_2 affects CdTe and CdS can be expected with either processing method.

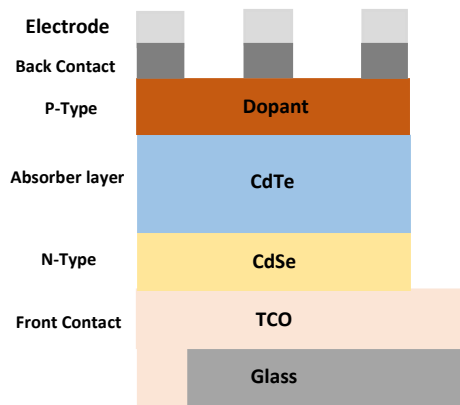


Figure 19: CdTe solar cell in superstrate configuration

3.8.5 Back contact and electrode

Graphite is typically used for the back contact. Graphene is adaptable and tunable for device layers. Graphite has a high carrier mobility, high thermal conductivity, great transparency and a high melting point. It is also a low cost method with great flexibility to fabricate devices. The electrode is responsible for collection. This also leads to overestimating the influence of back contact properties such as band offsets, barriers, and surface recombination on device performance. Typically, Cu or other elements like Mo, Au, Ag and others are used to dope the back contact and reduce the barrier height associated with carrier collection which will essentially enhance carrier collection and the PCE%.

3.9 Films and device characterization

The film thickness was determined by the surface profilometer (Dektak II). The structure of the grown films was performed by an X-ray Diffraction System (X'Pert). The film morphologies and chemical composition were determined by the scanning electron microscope (SEM, JEOL 7000) with Electron-dispersive Spectroscopy (EDS) attached to the SEM. The Raman experiments were conducted on a single stage Raman spectrometer with a solid-state laser (Horiba Lab Ram HR, 532 nm wavelength). The absorbance and transmittance spectra were measured using a UV-Vis spectrometer (Shimadzu UV-1800). The AFM and conductive AFM images were recorded on a grounded Sb_2Se_3 sample using an atomic force microscopy (AFM, Park XE70).

The current-voltage (I - V) curve of the solar cells were characterized using a solar simulator (Newport, Oriel Class AAA 94063A, 1000 Watt Xenon light source) with a source meter (Keithley 2420) at 100 mWcm^{-2} AM 1.5G irradiation. A calibrated Si-reference cell and meter (Newport, 91150V, certificated by NREL) was used to calibrate the solar simulator prior to cells measurement. External quantum efficiency (EQE) data were characterized by a solar cell spectral response measurement system (QE-T, Enli Technology, Co. Ltd). The solar cell device simulation was performed using the solar cell capacitance simulator (SCAPS) simulation¹¹¹.

(a)



(b)



Figure 20: (a) Solar cell current-voltage (I-V) characteristic measurements (b) Solar cell external quantum efficiency (EQE) characteristic measurements

3.9.1 Current-voltage (I-V)

The current-voltage (I-V) curve tells us the direct relationship between direct current through a device and the voltage across its terminal. The curve is typically used to determine basic parameters of device performance like open circuit voltage (V_{oc}), short circuit current (J_{sc}) and the fill factor (FF) that is used to model the behavior of devices for further improvements. The solar simulator is shown in Figure 20a, this solar simulator with I-V measurement capabilities was used to characterize all cells in this study.

3.9.2 External quantum efficiency (EQE)

The external quantum efficiency applies to incident photon that may be absorbed or reflected from the surface. The EQE curve determines of all the incident light that hit the surface, how much of this light has been absorbed and how much of this light has been reflected off the front and back surface. Typically the back surface recombination is low. The front surface recombination gives an idea of how many photons are reflected off the surface. Knowing this information will give a better idea on how to engineer new architectural designs that would further eliminate the effects of front surface recombination. In addition, the EQE curve also gives an idea of how strong the diffusion length is for minority carriers. The EQE characteristic measurement device is shown in Figure 20b, this measurements was used to characterize all cells in this study.

3.9.3 Capacitance-voltage (C-V)

C-V characteristics are typically used to characterized the junction of the solar cell in reverse bias⁵⁵. Applying a voltage in reverse results in a disruption of carrier balance between

drift and diffusion carriers at the junction. In reverse bias, when the voltage is applied across the solar cell so that the electric field formed at the p-n junction is increased¹¹². Here, the diffusion current decreases because the electric field at the junction increases which lowers the probability that carriers can diffuse from one side of the junction to the other. Extracted minority carriers are generated at the surface and the diffusion current decreases¹¹². Reverse current is smaller than the forward current because there are fewer carriers available for extraction. In semiconductor devices, C-V measurements can reveal oxide thickness, oxide charges, surface contamination and trap densities^{112, 113}.

CHAPTER 4

SOLUTION-PROCESSED COPPER (I) THIOCYANATE (CUSCN) FOR HIGHLY EFFICIENT CdSe/CdTe THIN FILM SOLAR CELLS

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Solution-processed CuSCN serving as a hole transport (HTL) and a Cu dopant source for CdSe/CdTe thin-film solar has demonstrated with a high power conversion efficiency (PCE) of ~17%. Two types of solvents were used in this work, diethyl sulfide (DES) and aqueous ammonia (NH₄OH), are explored as solvents used to deposit CuSCN on CdTe. Both solvents have the ability to enhance the performance of CdSe/CdTe solar cells, however; NH₄OH solvent is less toxic, less expensive and leads to a smoother film surface in comparison to the DES solvent. NH₄OH films fabricated allowed for an ultra-thin deposition of the CuSCN layer while also avoiding the high cost associated with DES. Temperature-dependent current voltage (J-V-T) and temperature dependent capacitance-voltage (C-V-T) measurements reveal that the use of CuSCN as a HTL increases carrier concentration in the CdTe absorber and significantly reduces back-contact barrier height which ultimately improves carrier transport. A high power conversion efficiency is achieved with an optimal thickness of the CuSCN layer. Our results show the promise of solution processed CuSCN HTL for enhanced efficiencies and reduced costs for an improved CdTe thin-film solar cell

4.1 P-Type doping: Group 1 dopant

4.1.1 Copper (Cu) doping

The significance of doping Cu in CdTe solar cell absorber layer has shown to be one of the most promising avenues taken to enhance p-type doping in CdTe solar cells. Models have been shown that express a deeper understanding in the case of Cu doping in CdTe solar cells. An optimum Cu concentration is needed to maximize device performance. The concentration of Cu is so important because it determines how much Cu can diffuse into the adsorbed layer leading to device improvements. The conductivity is also determined by the concentration of Cu, if the Cu concentration is too high, this would lead to higher resistivity in the device which would hinder carrier transport and lower the conductivity. In addition, if the Cu concentration is too high, this would lead to a metal-to-insulator transition where too many dopant atoms are moving through the lattice at long distances without changing their energy, which leads to an insulating behavior. To the contrary, if the Cu concentration is too low, this would lead to low solubility that promotes accumulation of elements at the grain boundary as well as the interfaces of the device. In addition, high compensational issues that would hinder the lifetime of carriers will arise with low concentration devices. Traditionally, CuCl_2 is used as a dopant source by using a dry physical vapor deposition (PVD) method. Most methods used perform a single role of Cu dopant incorporation by means of some PVD method. The challenge here is the ability to accurately control the Cu concentration during and after dopant activation. In addition, PVD methods cost more which could lead to undesirable manufacturing costs. Moreover, Cu has been used to substitute the back contact to form an ohmic contact in CdSe/CdTe devices that would lower the barrier height and enhance carrier collection to the back contact. Much improvement has been shown on doping the back contact with Cu constituents, however; more

complex manufacturing is needed for the incorporation of Cu, plus Cu oxidizes into a porous compound when exposed to air which leads to degradation. However, excess Cu concentrations can form Cu_i which act as a shallow interstitial donor defects that could lead to the compensation of Cu_{Cd} . In addition, because the atomic radius of Cu is small, it also diffuses rapidly in CdTe and reduces the minority carrier lifetime. Therefore, optimum amount of Cu is necessary to achieve best device performance. Recent studies suggest that intrinsically p-type CdTe could suffer from low minority carrier lifetime because of the formation of substitutional and interstitial midgap defects. This means, even if a higher carrier concentration is achieved for extrinsically-doped p-type CdTe, poor carrier lifetime would limit the V_{oc} ¹¹⁴.

4.1.2 Solvent processed CuSCN

In this study, we applied solution-processed CuSCN as hole transport layer (HTL) for the CdSe/CdTe thin-film solar cells using DES and an aqueous NH_4OH solution as solvents used in the precursor. The improved V_{oc} and FF for the CdSe/CdTe solar cells with the solution-processed CuSCN lead to 17% PCE with reduced series resistivity by CuSCN thickness and concentration optimization. The improved device performance benefits from CuSCN for high V_{oc} and FF, while CdSe window layer accounts for high J_{sc} contributes the efficiency improvements. Temperature-dependent current-voltage and capacitance-voltage measurements reveal that the use of CuSCN HTL increases hole (carrier) concentration in the CdTe absorber layer which can significantly reduce the back contact barrier height and improve carrier transport. The CdTe devices fabricated with the aqueous NH_4OH -based CuSCN precursor solution showed similar devices performances to that of DES-based CuSCN precursor solution. The cost-effective solution-processed CuSCN for CdTe devices provides a promising pathway to

reduce the cost of solar energy technology production and other associated cost of manufacturing.

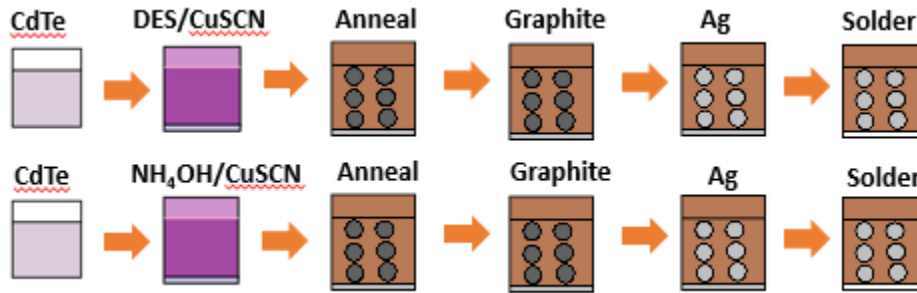


Figure 21: CuSCN was deposited the same way using diethyl Sulfide (DES) and an aqueous ammonia hydroxide (NH₄OH) solutions were chosen as solvents

The deposition of DES/CuSCN and NH/CuSCN is shown in Figure 21. The process looks similar but the control of the Cu concentration through careful fabrication and cell architecture was essential in optimizing device performance. To further achieve a higher PCE% of CdTe solar cells, a higher open circuit voltage (V_{oc}) and fill factor (FF) are required. Traditionally, to improve the V_{oc} , Cu doping is used as an affordable and effective way to fabricate high efficiency CdTe devices. Recently, other strategies have been proposed and demonstrated successfully to improve V_{oc} . For example, a higher open circuit voltage (V_{oc}) of above 1.0 V in monocrystalline CdTe with a PCE ~17% by doping with phosphorus (P) has been achieved⁹⁸. However, polycrystalline CdTe devices with 22% PCE suffers a relatively low V_{oc} close to 0.9 V⁸³. It is a huge challenge to introduce P or other group V dopants (eg, As and Sb) into the polycrystalline CdTe to further improve the V_{oc} ¹¹⁵. Thus, an alternative way to further improve the V_{oc} is to applied in this work. Traditionally, other hole transporting layers (and/or electron reflecting layer (ERL)) is used to improve the carrier collection function to the back contact. Various inorganic and organic hole transport layers have been employed on CdTe devices to increase carrier concentration including; Cu doped ZnTe, P3HT, PEDOT:PSS, and Sprio-

OMeTAD¹¹⁶⁻¹¹⁸. However, depositing these functional layers may need expensive physical vapor deposition (PVD) facilities. To further reduce the cost of the solar cells, an affordable and effective solution process to integrate these functions into one layer (i.e, hole transport layer, electron blocking layer, and doping) is desired.

Copper thiocyanate (CuSCN) is an inexpensive inorganic material with promising electronic property (i.e, high work function ~5.3 eV) and optical properties (i.e, bandgap ~3.6 eV), that has been investigated for several decades¹¹⁹. CuSCN is an inorganic stable material that is commercially available. CuSCN has an optical transparency and it is non-toxic leading to an efficient HTL for low temperature processing. This method is simple and a robust dopant source which could be a good replacement for traditional methods like Pedot:PSS or SPIRO-OMeTAD that are organic compounds known to degrade in air. More recently, CuSCN has made a promise at being a cost-effective hole transport layer (HTL) for perovskite solar cells which has achieved an PCE ~20% using a solution-processed procedure¹²⁰. Meanwhile, CuSCN was also used for other dye-sensitized solar cells (DSSC) such as chalcogenides Sb₂S₃^{121, 122}. For CdTe solar cells, physical vapor deposited CuSCN thin film has also been investigated to improve the V_{oc} for CdS/CdTe devices¹²³.

Although, it is challenging for solution-processed CuSCN (~100 nm) to achieve a thin layer compared with the vapor process counterparts (~10 nm) in CdS/CdTe devices, it is well deserved to try to tailor the solution-processed CuSCN on CdTe devices considering that CuSCN uniquely combines desirable characteristics as a Cu doping source for CdTe p-type doping, a desired hole extraction, and an electron reflecting behavior. In particular, an aqueous CuSCN precursor solution for CdTe is even more promising to be integrated into the ambient solution process for a high-throughput manufacturing. Traditionally, diethyl sulfide (DES) is typically

used for dissolving CuSCN. Still, the DES-based CuSCN layer is difficult to get an ultra-thin and smooth layers due to high viscosity and rough topography of DES expressed in other studies¹²³.¹²⁴ Recently studies have shown that using aqueous ammonia (NH₄OH) as a solvent for CuSCN precursor solution can achieve a relatively thin layer (5-10 nm) with smooth topography and successfully utilized to obtain PCE ~17%.

4.1.3 Experimental details

CuSCN (99% Sigma-Aldrich) was dissolved into diethyl sulfide (DES, 98%, Sigma Aldrich) and aqueous ammonia (NH₄OH, 28% Alfa Aesar) at a concentration of 10 and 20 mg mL⁻¹, respectively. The solutions were magnetically stirred at room temperature for 5 hours to become fully dissolved and filtered using a 0.45- μ m pore size PTFE filter prior to the thin film spin coating deposition. The CuSCN thin-film was deposited by spin coating with tunable rotation speed (1000 to 8000 rpm) to control the film thickness for 30 seconds.

4.1.4 Solar cell characterization

The AFM and the EFM were conducted using atomic force microscopy (AFM, Park XE70) using a Pt/Ir coated contact probe (ANSCM-PT from AppNano, Inc). The cantilever spring constant was about 3 N/m, and resonance frequency was at around ~60 kHz. The current-voltage (J-V) curve of the solar cells was characterized using a solar simulator (Newport, Oriel Class AAA 94063A, 1000 Watt Xenon light source) with a source meter (Keithley 2420) at 100 mW cm⁻² with AM 1.5G irradiation. A calibrated Si-reference cell and meter (Newport, 91150 V, certificated by NREL) was used to calibrate the solar simulator prior to cells measurement. External quantum efficiency (EQE) data were characterized by a solar cell spectral response measurement system (QE-T, Enli Technology, Co Ltd). Temperature-dependent current-voltage (J-V-T) and capacitance-voltage (C-V-T) measurements were performed using a Solartron

Modulab potentiostat equipped with a frequency response analyzer (Ametek Inc). The J-V-T measurements were performed in dark with DC voltage sweeping from -0.4 to 1.5 V. The C-V measurements were performed in the dark with a constant modulation voltage 45 mVrms and frequency of 10 kHz. AC signal superimposed on a DC bias voltage varying from 2.0 to 0.5 V. A liquid-nitrogen cooled cryogenic system (Janis VPF-100) was used to carry out all temperature dependent (150 to 300 K with a step size of 10 K) measurements. The temperature was controlled by a temperature controller (Lakeshore 330). A temperature sensor was mounted on the top of the device directly to ensure that the recorded temperature is the correct device temperature.

4.1.5 Solar cell fabrication

The CdTe film with $\sim 3\mu\text{m}$ was deposited on the sputtered CdSe (~ 100 nm) buffered F-doped SnO_2 (FTO, NSG USA) substrate using the close-space sublimation (CSS) method. The detailed CSS deposition process was reported elsewhere¹²⁵. The CdTe films were thermally treated using the CdCl_2 solution at 400°C for 20 to 30 minutes in the ambient air. The CdTe surface was rinsed using deionized water (DIW) to remove the residual CdCl_2 , following an etching process using the diluted HCl solution to remove the surface oxides layer before the coating and back contact deposition of CuSCN. For DES-based CuSCN, the solution was denoted as DES-CuSCN, and for NH_4OH -based CuSCN, solution was denoted as NH-CuSCN. The thickness of the DES-CuSCN and NH-CuSCN layers was 30 to 60 nm and 10 to 20 nm, respectively. The thickness was tuned through the spin coater rotation speed. Thicknesses was measured using a Stylus profiler (Dektak II). The back contact for the CdTe cells was screen-printed using graphite and silver (Ag) paste. The cells area is 0.08 cm^2 . The cells were heat

treated for about 20 minutes at 200°C to drive the Cu concentration into the CdTe for increased carrier collection.

4.1.6 Device performance

The improved device performance is known to be contributed from the benefits of a high V_{oc} and FF, while the CdSe window layer provides a high J_{sc} that contributes to higher carrier transport and efficiency improvements. The CdTe devices performed with the aqueous NH_4OH based CuSCN solution has shown similar devices performances to that of DES-based CuSCN. The cost-effective solution processed method used to fabricate CdTe using CuSCN as a HTL and Cu doping source for devices improvements provides a promising pathway to reduce the cost of solar energy.

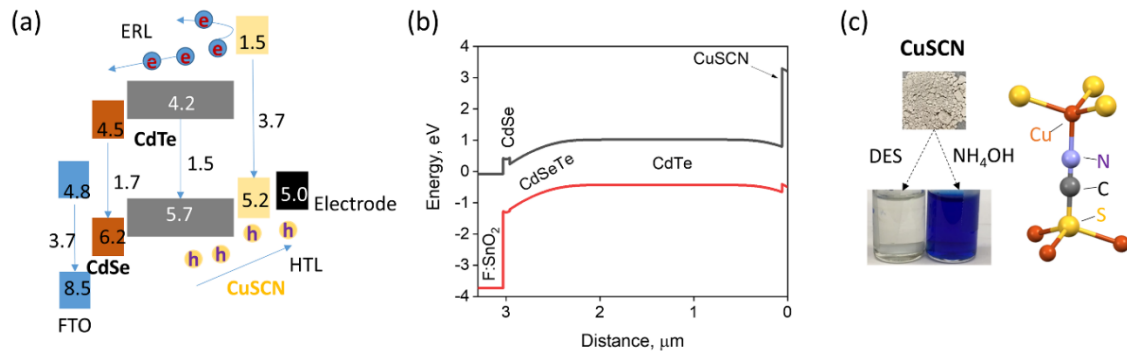


Figure 22: (a) The energy level diagram of each layer in the FTO/CdSe/CdTe/CuSCN/graphite solar cells. (b) SCAPS modeling determined energy band diagram of the solar cells. (c) CuSCN powder dissolved into DES and NH_4OH , respectively

The CuSCN chemical structure is shown in Figure 22a, the energy level diagram of the FTO/CdSe/CdTe/CuSCN/graphite shows how CuSCN combines the hole transport layer (HTL) with the electron reflecting layer (ERL) and plays as a dual role based on the energy bandgap edge offset with respect to that of CdTe. The solar cell device simulation was performed using the solar cell capacitance simulator (SCAPS) simulation and it is shown in Figure 22b indicating

the bandgap diagram calculated using this SCAPS modeling¹¹¹. SCAPS is a one-dimensional solar cell simulation program used to simulate different performance properties using different semiconductor layer thicknesses. The thickness of CuSCN directly impacts carrier transport to the back contact due to the high resistivity that can play as a barrier for carrier transport when too thick¹²³. Figure 22c show the two solvents used in this work that is responsible for tuning the thickness of the CuSCN layer. The CuSCN precursor made from the dissolved DES is transparent which corresponding to its wide bandgap (~ 3.6 eV), where the CuSCN precursor made from NH₄OH solution is a dark blue color, this is associated with the (Cu(NH₄)₂)⁺ complex formation formed while making the precursor¹²⁶⁻¹²⁸. In both cases, the final CuSCN film (after extraction of the solvent) is transparent because of its large bandgap. The chemical structure of inorganic CuSCN is presented in Fig. 22c, where the Cu ions are split by the SCN ions and a strong Cu-S bond that interconnects three-dimensionally. The structure also makes CuSCN a Cu source for CdTe Cu doping, which is a necessary process to improve the V_{oc} in CdTe devices¹²⁹. Thus, CuSCN used for CdTe devices plays a multi-roles to engineer the device performance. In addition, because of the toxic nature of elemental CdTe, the pre-deposited CdTe samples were prepared in collaboration with colleagues. The CdTe films were cleaned thoroughly and dried using the ozone to remove any unwanted water molecules and other contaminants from the surface of the CdTe which leads to an ultra-clean surface preparation for device fabrication. The precursor was used in the dopant deposition step and performed via solution based method on an accurate speed and time to ensure full uniformity and deposition throughout the entire cell. Solar cell fabrication and activation was performed to ensure controlled activation though an intensive low temperature heat treatment. Cell measurements were then performed.

4.1.7 Film morphology

To understand the interface quality and surface electronic behavior between the DES and NH_4OH based CuSCN on the CdTe surface, the atomic force microscopy (AFM) and electrostatic force microscopy (EFM) were carried out. The AFM and the EFM were conducted using atomic force microscopy (AFM, Park XE70) using a Pt/Ir coated contact probe (ANSCM-PT from AppNano, Inc). The cantilever spring constant was about 3 N/m, and resonance frequency was at around ~ 60 kHz. The CuSCN layers were spin coated on the etched CdTe surface. The bare CdTe surface without CuSCN is shown as a reference in Figure 23a, c, e for AFM morphology and Figure 23b, d, f shows EFM amplitude, respectively.

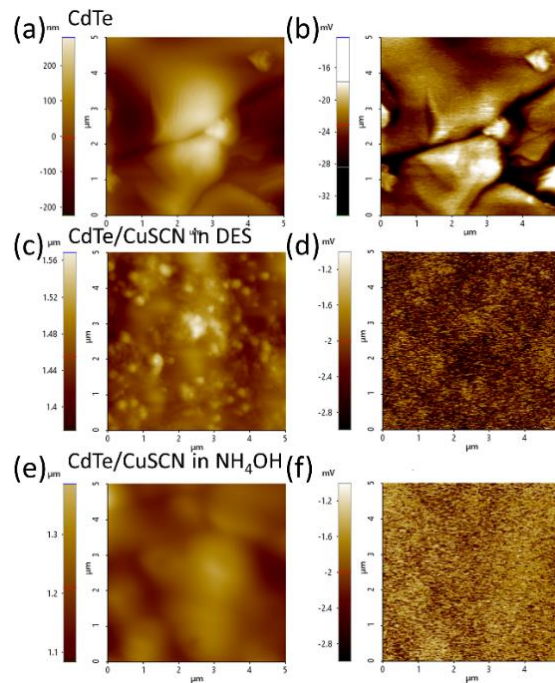


Figure 23: (a), (c) (e) Atomic force microscopy (AFM) surface morphology images, and (b), (d), (f) Electrostatic force microscopy (EFM) amplitude images of bare CdTe, DES/CuSCN and NH_4OH /CuSCN coated CdTe, respectively. ($5 \times 5 \mu\text{m}^2$)

The CdTe grain size is in the micrometer level (e.g., 2~3 μm). In the EFM amplitude image, the grain boundary shows relative lower electrostatic force value compared to the grain, suggesting that the Cl passivation at the grain boundary after CdCl₂ heat treatment.¹²⁵ Figure 23d-e show the AFM morphology and EFM amplitude images for the DES/CuSCN, respectively. The DES/CuSCN particles in nanoscale (~ 50-100 nm) can be observed with a surface root mean squared (RMS) roughness of ~ 7 nm (Fig. 23d), which is consistent with the DES/CuSCN coated on the glass substrate.¹²⁶ The EFM images in Fig. 23e shows that the electrostatic force on the DES/CuSCN can significantly reduce the surface charges on the CuSCN. The electrostatic amplitude was reduced one order of magnitude (CdTe/CuSCN surface ~ 2 eV vs. bare CdTe surface ~ 24 eV, as shown in Fig. 23b, which suggests that the CuSCN layer is highly resistive and can prevent the electron transport through the back contact (i.e., electron reflecting role). NH/CuSCN film is much smoother morphology with RMS ~ 1.2 nm than that of the DES/CuSCN, and the electronic surface is more uniform. This smoother surface of NH/CuSCN can planarize the rough bare CdTe surface and provide better contact with the back contact. Meanwhile, the NH/CuSCN film shows similar electronic behavior as that of the DES/CuSCN, also could reduce the reflecting the electron transport in the back contact. With the aqueous NH₄OH as a solvent for CuSCN, it is more convenient to tailor the thickness of CuSCN than that of DES solvent.

4.1.8 Results

4.2.1 Device performance from DES/CuSCN on CdTe devices

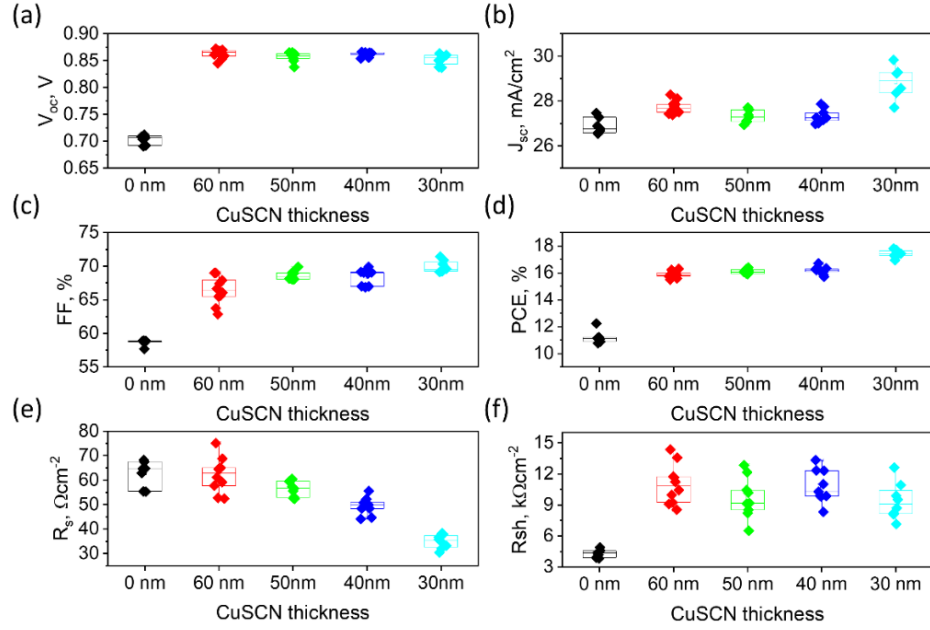


Figure 24: Statistical distribution of (a) V_{oc} , (b) J_{sc} , (c) FF , (d) PCE , (e) R_s , and (f) R_{sh} of CdTe solar cells based on CuSCN from DES solution. The cell performance data were selected for 10 cells for each CuSCN thickness

Figure 24 shows the device performance for the DES/CuSCN based CdSe/CdTe solar cells with tuning the CuSCN thickness. It is reported that the sputtered CuSCN thickness can influence the CdS/CdTe devices performance remarkably, in particular, will improve the V_{oc} , and reduce the fill factor (FF).¹²³ Without CuSCN (i.e., 0 nm, means no HTL, ERL and Cu doping), the CdSe/CdTe device PCE is $\sim 11\%$, $V_{oc} \sim 0.7$ V, $J_{sc} \sim 26.5$ mAcm⁻² and the Fill factor (FF) $\sim 58\%$, which is similar with the CdS/CdTe devices without CuSCN¹²³.

The CdTe devices without the Cu doping show a power conversion efficiency about 10% and with low $V_{oc} \sim 0.7$ V and this is expected since there is limited carrier concentration due to Cu-free in the devices. With the CuSCN doping, the V_{oc} was significantly improved as shown in Fig. 24 a. We systematically did a device characterization of cells through the current-voltage curves. Each condition has around 10 cells and plotted statistically to show the distribution about

these cells device performances. The improved J_{sc} compared to the CdS/CdTe device is due to the CdSe window layer can be consumed by CdTe to form into $CdSe_xTe_{1-x}$ absorber, which can absorb more short and long wavelength sunlight spectrum.^{109, 130} The dominated cause for the inefficient device performance is associated with the high series resistivity (R_s), and low shun resistivity (R_{sh}), as shown in Fig. 24e-f. With the introduction of CuSCN layer, the PCE of CdSe/CdTe device can be boosted to 16% with 60 nm thick DES/CuSCN layer. The increase for the device parameters can reach $V_{oc} \sim 0.855$ V, and $J_{sc} \sim 27.5$ mAcm⁻², and FF $\sim 67\%$. This device performance improvement origins from the hole extrusion role and Cu doping effect from CuSCN. The incorporation of the CuSCN is also expected to be an electron reflecting layer due to its wide bandgap, high conduction band minimum (CBM), as shown in Fig. 24a-b. However, the series resistivity, R_s is still high and similar to that of the CdTe without CuSCN. This is expected because the high resistivity of the thicker CuSCN layer prevent the carrier transport.¹²³ All high efficiency solar cells to date use Cu doping.

Even though the mobility of interstitial Cu is extremely high which would affect the device performance, promising results have been shown through modeling and experimental studies that show the ability of Cu doping on increasing carrier concentration and the lifetime of carriers. Controlled amounts of Cu have led to a record breaking laboratory efficiency in CdTe devices of 22.0% PCE²⁷. Cu plays two important roles in CdTe devices. Cu can either occupy vacant Cd sites to form a substitutional acceptor defect Cu_{Cd} . In this case, Cu will occupy the V_{Cd} site in intrinsically doped CdTe to form Cu_{Cd} and due to the low formation energy of V_{Cd} compared to V_{Te} , CdTe is an intrinsically p-type semiconductor¹³¹. Interstitial Cu diffuses fast and accumulates at the interfaces of CdTe/CdS solar cells and is believed to be the main reason for degradation and instability in CdTe devices. Studies have shown that excess Cu has

unwanted effects on the minority carrier lifetime in CdTe⁹⁴. Cu as a group I impurity continues to play a key role in CdTe devices and is expected to exhibit a better lifetime in doping heterojunction CdSe/CdTe solar cells.

4.2.3 I-V and EQE on CuSCN using DES

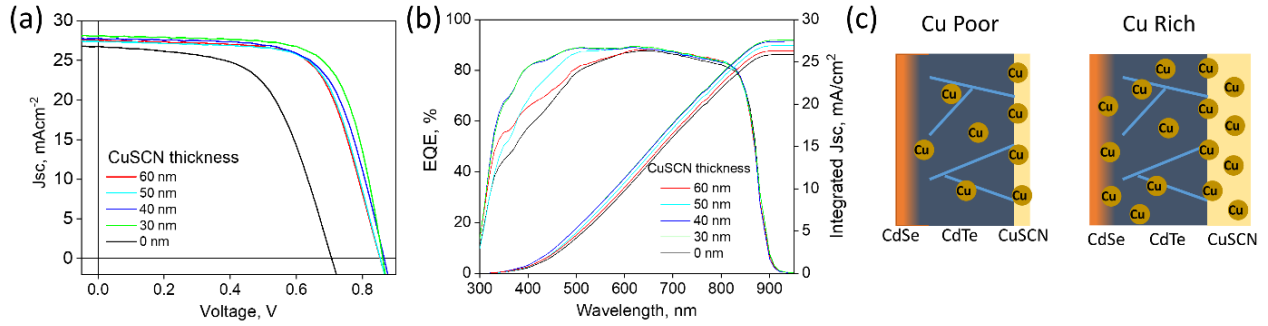


Figure 25: (a) I - V curves and (b) external quantum efficiency (EQE) spectra of the champion CdTe cells with various thicknesses of DES/CuSCN. (c) the schematic of the Cu concentration in the CdTe solar cells with varying CuSCN thickness

Figure 25a, b shows the J - V curve and external quantum efficiency (EQE) curve for the champion cells with various DES/CuSCN thickness, respectively. The thickness of the DES/CuSCN significantly impacts on the blue response (short wavelength < 500 nm). Since the CdTe films were experienced in the identical CdCl₂ treatment, thus we assume that the impact of the CdSe window layers impact for the EQE response may not dominate the front interface absorption. However, the different consumption level of the CdSe window layer post he CdCl₂ treatment, e.g., to form the CdSeTe ternary absorber layer, may still be different considering that the nonuniformity of CdTe film, which may impact the front interface transmittance.

Here, we focus on the DES/CuSCN thickness influence for the EQE. The thinner the DES/CuSCN layer, the higher the conductivity of DES/CuSCN and the better the J_{sc} determined from the EQE curves, as shown in Fig. 25b. This can be ascribed to the front contact Cu

concentration may be increased with increasing the DES/CuSCN thickness during the back contact heat treatment. This will influence front contact light absorption at the short wavelength region.¹²⁹ As shown in Fig. 25c, the thin DES/CuSCN may provide the desired Cu concentration in the CdTe devices, however, in a thick DES/DCuSCN layer, the Cu may diffuse into front contact which will damage the front contact absorption. Thus, the thickness of the CuSCN not only impact the V_{oc} due to CuSCN high resistivity but also impact the J_{sc} due to the Cu doping and manipulated transmittance of the front interface.

4.2.4 Device performance from NH/CuSCN on CdTe devices

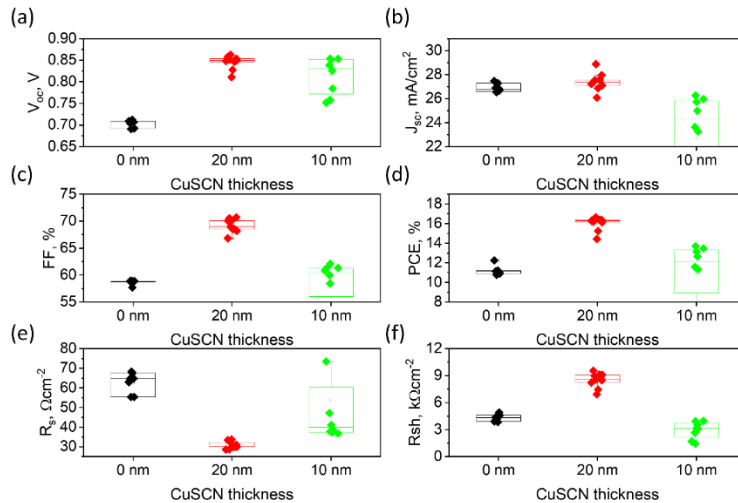


Figure 26: Statistical distribution of (a) V_{oc} , (b) J_{sc} , (c) FF , (d) PCE , (e) R_s , and (f) R_{sh} of CdTe solar cells based on NH/CuSCN layer. The cell performance data were selected for 10 cells for each NH/CuSCN thickness

To further reduce the CuSCN thickness, we explore the CdTe device performance using the NH_4OH based CuSCN. It is successful to achieve 10 nm and 20 nm thick NH/CuSCN via tuning the rotation speed of NH/CuSCN solution. Figure 26 shows the device performance for the NH/CuSCN in 10 and 20 nm thickness with a comparison of the bare CdTe device. With respect to the bare CdTe devices without CuSCN, the champion PCE of CdSe/CdTe device with

20 nm NH₄OH based CuSCN can achieve $V_{oc} \sim 0.85$ V, $J_{sc} \sim 28.4$ mAcm⁻², $FF \sim 70\%$ and leads to PCE $\sim 16.39\%$, which is close to the best CdTe device with DES/CuSCN (17.03%).

However, the solar cell parameters for the 10 nm NH/CuSCN is lower than that of 20 nm NH/CuSCN. This could be due to the insufficient Cu doping level using this 10 nm thick CuSCN layer. The low Cu concentration impact can also be observed from the improved series resistivity and the reduced shunt resistivity for this 10 nm thick NH/CuSCN. In addition, the device parameters of CdSe/CdTe solar cells with thin NH/CuSCN layers show narrow spreading in the R_s and R_{sh} , while more scattering in V_{OC} , FF , and J_{sc} , which could be associated with the thickness dependent resistivity of CuSCN layer, the high roughness of the CdTe film with larger grain size and topographical grain height. For example, 20 nm thick NH/CuSCN could provide sufficient Cu doping but may not provide uniform coverage on the rough CdTe back surface. In contrast, the device parameter of the thicker DES/CuSCN covered CdSe/CdTe devices could provide better surficial coverage, however, the resistivity of thicker CuSCN could impact the R_s and R_{sh} significantly and then impact on the carrier collection.

4.2.5 I-V and QE on CuSCN using DES

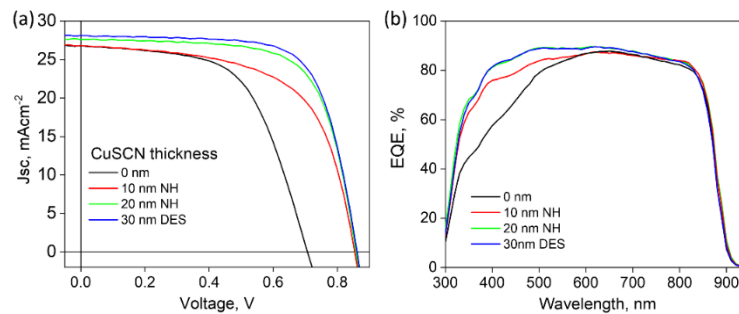


Figure 27: (a) J-V curves and (b) external quantum efficiency (EQE) spectra of the best performing CdTe cells with NH/CuSCN. The best CdTe device performance with DES/CuSCN is also included for comparison

As shown in Figure 27, both the DES/CuSCN and NH/CuSCN coated CdTe device performance are plotted together for the champion cells. It is demonstrated that both solvents for CuSCN could provide sufficient Cu doping in CdTe with tailoring the thickness of CuSCN to tune the Cu concentration and CuSCN resistivity. Considering the DES more expensive than NH₄OH, it is more desired to use aqueous NH₄OH as a CuSCN solvent. The champion devices parameters for DES and NH₄OH solvents based CuSCN coated CdTe devices are listed in Table 1, where their V_{oc} is almost identical, while the J_{sc} and FF for the NH/CuSCN coated CdTe device still need to be improved with optimization of the CuSCN thickness and concentration.

Table 2. Device parameters of champion CdTe cells with CuSCN from DES and NH₄OH solvents, respectively.

CuSCN solvent	V_{oc}, V	$J_{sc}, mAcm^{-2}$	$FF, \%$	$R_{oc}, \Omega cm^2$	$R_{sh}, \Omega cm^2$	PCE, %
DES	0.860	28.16	70.31	33.2	10933	17.03%
NH₄OH	0.858	27.65	68.97	33.4	9521	16.36%

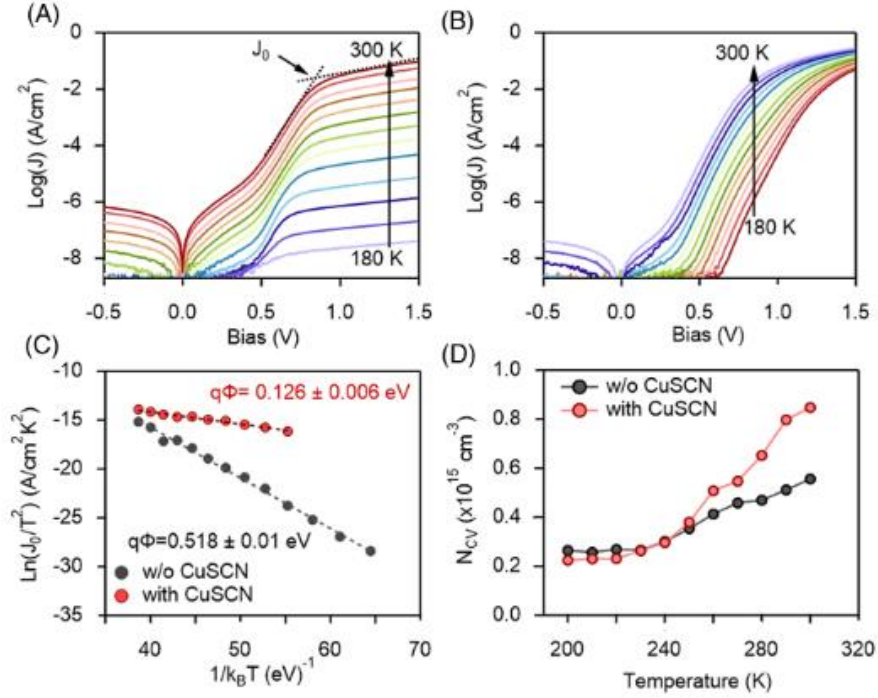


Figure 28: Dark J-V-T curves of the CdTe devices a, without and b, with CuSCN layer. c, Arrhenius plots that were used to calculate back-contact barriers ($q\Phi$). d, Carrier concentration as a function of temperature of both devices that are calculated from the fitting curve of Mott-Schottky plots

J-V-T measurements were carried out for CdTe cells with and without CuSCN HTL to understand the effects of CuSCN HTL (Figure 28a, b). J-V diode behaviors were observed from both devices at room temperature. However, cooling the device without CuSCN to lower temperatures led to a rollover at forward biases, indicating non-ohmic contact at the CdTe/back contact interface. However, such rollover is significantly suppressed in the device with CuSCN HTL. We further extracted the activation energy (E_a) for the back-barrier using an Arrhenius plot of $\ln(J_0/T^2)$ versus $1/k_B T$, as shown in the insets of Figure 28c. The back barrier height is measured to be 0.578 eV for the cell without CuSCN, but it is significantly reduced to 0.126 eV for the cell with CuSCN, partially responsible for the improved FF. We further calculated carrier concentration (N_{cv}) based on Mott Schottky plots and C-V-T measurements. As shown in Figure

28d, at room temperature, the hole density in the absorber of the device with CuSCN HTL is higher than in the device without CuSCN HTL. It is reasonable to consider that the increase of hole density is due to Cu diffusion from CuSCN HSL into CdTe layer.

4.3 Fabrication challenges

It is a challenge for the DES/CuSCN to become thinner.¹²⁴ Here, we tailor the DES/CuSCN thickness from 60 to 30 nm with increasing the spin coating speed. With decreasing the DES/CuSCN thickness, it is shown that the R_s decreased gradually which leads to the remarkable improved FF to 71% for 30 nm thick DES/CuSCN. Meanwhile, the J_{sc} also was improved to 29 mAcm⁻² with DES/CuSCN thickness of 30 nm compared to the 27.5 mAcm⁻² of 0 nm CuSCN. The improved J_{sc} with a change of DES/CuSCN thickness is also associated with the Cu concentration and CdSe thickness variation at the front interface in CdSe/CdTe devices, which was confirmed by the EQE measurements later. Thus, the champion device's PCE of 30 nm DES/CuSCN was achieved to be 17.03% with the improved J_{sc} , and FF. However, the V_{oc} kept stable ~ 0.855 V with varying the CuSCN thickness, which could be associated with the Cu concentration may be saturated at 30 nm DES/CuSCN. In addition, it is also observed that the J_{sc} at 30 nm CuSCN shows larger spreading than that of thicker DES/CuSCN, this may be due to the nonuniformity of DES/CuSCN coated on the CdTe surface as shown in AFM topography (Fig. 23c). The nanocrystalline CuSCN may embed into the back contact and impact the current collect during the J - V measurement.

4.4 Copper (Cu) conclusions

Cu doping using CuSCN as a dopant source has allowed for an increase in device performance of up to 17% PCE. Unfortunately, because Cu diffuses fast in CdTe sublattice this could lead to future undesired degradation in device performance. In addition Cu has been shown

to diffuse through to the junction of CdS/CdTe forming detrimental recombination centers that shunt carrier pathways and limit the lifetime of carriers. The literature often compares Cu to Ag in an effort to analyze theoretical and experimental the advantages and disadvantages of both dopants.

4.5 Silver (Ag) doping

Controllable extrinsic doping depends strongly on the stoichiometry and background impurities in semiconductors. Crystal growth requires high temperatures and silver (Ag) dopants are assumed to act as a substitutional acceptor (Ag_{Cd}) or as an interstitial donor (Ag_i). In the early years of Ag doping in CdTe, J. Hamann *et al.* verified the identity of the substitutional acceptor (Ag_{Cd})¹³². Then J. Bollmann *et al.* showed that p-type Ag dopants would be interstitial atoms and may form neutral complexes with shallow acceptors. They also showed the Ag_i cannot be a shallow donor because of self-compensation. Then H. Wolf and colleagues *et al.* produced a model to describe the diffusion profiles of Ag in CdTe. Their model showed that Ag_i and Ag_{Cd} is caused by drift mechanism in intrinsic and extrinsic semiconductors¹³³. S. Ding and colleagues *et al.*¹³⁴ studied the effect of Ag doping in CdTe and compared that to the case of Cu doping. They showed the minimum resistivity and maximum hole density is achieved using Ag. They also found that Ag doping caused a strong compensational effect when the optimum maximum dopant amount was reached. N. Abbas *et al.* showed the mobility of holes and carrier concentrations increased during Ag doping and that the conductivity increased as a function of temperature. In addition, a shape and size change of the CdTe grains were observed as well¹³⁵. In 2002, S. Huai *et al.* and colleagues used first principle calculations and found that Ag and P are likely to be the best p-type dopants after calculating the formation energies and transition energy levels of intrinsic and extrinsic defects in CdTe⁹⁴. High recombination sites can limit carrier

concentration through the junction and degrade the optoelectronic properties, in fact; J. Tregilgas et al.¹³⁶ observed how Ag impurities migrate up a concentration gradient and segregate near the surface of p-type CdTe during the exposure to ambient air which is believed to be caused by the redistribution of positively charged interstitial Ag (Ag_i) impurities during doping.

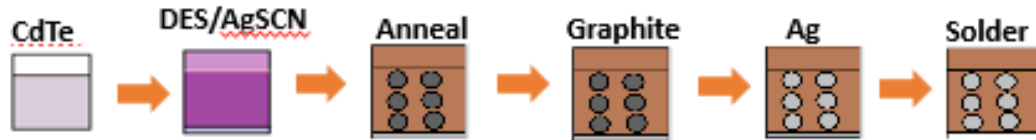


Figure 29: AgSCN was deposited using diethyl Sulfide (DES) was chosen as a solvents

The deposition of DES/AgSCN is shown in Figure 29. The process looks similar to that of CuSCN but the control of the Ag concentration through careful fabrication and cell architecture was essential in optimizing device performance. To further achieve a higher PCE% of CdTe solar cells, a higher open circuit voltage (V_{oc}) and fill factor (FF) are required. DES was chosen as a solvent in this study due to the results that were obtained using the CuSCN. We found that DES as a solvent has the ability to provide ultimate carrier concentration that further enhance device performance. The disadvantage to DES is that it cost more than the ammonia but it has produced higher PCE% than other solvents.

4.5.1 Solvent processed CuSCN and AgSCN

In this study, we compared our previously reported solution-processed CuSCN as hole transport layer (HTL) for the CdSe/CdTe thin-film solar cells using DES and compared it to AgSCN as solvents used in the precursor. The improved V_{oc} and FF for the CdSe/CdTe solar cells with the solution-processed AgSCN lead to 16% PCE. The improved device performance benefits from AgSCN for high V_{oc} and FF, while CdSe window layer accounts for high J_{sc} contributes the efficiency improvements. The CdTe devices fabricated with the aqueous DES-

based CuSCN precursor solution showed similar devices performances to that of DES-based AgSCN precursor solution. The cost-effective solution-processed AgSCN and CuSCN for CdTe devices provides a promising pathway to reduce the cost of solar energy technology production and other associated cost of manufacturing.

4.5.2 Experimental details

In this study, the CdTe solar cells were fabricated by CSS on the commercial TEC15 (Fluorine doped SnO₂ coated soda lime glass, NSG, USA). The CdSe window layer was deposited using a magnetron sputtering system with a CdSe target. The detailed window and absorber layer deposition conditions were described elsewhere^{91, 109}. AgSCN (99% Sigma-Aldrich) was dissolved into diethyl sulfide (DES, 98%, Sigma Aldrich) and aqueous ammonia (NH₄OH, 28% Alfa Aesar) at a concentration of 10 and 20 mg mL⁻¹, respectively. The solutions were magnetically stirred at room temperature overnight and filtered using a 0.45 μm pore size PTFE filter prior to the thin film spin coating deposition. The CuSCN thin-film was deposited by spin coating with tunable rotation speed (1000 to 8000 rpm) to control the film thickness for 30 seconds. The thickness of the CuSCN and AgSCN was controlled by using the spin coating conditions with a fine tune of around 30 nm for each layer.

The current-voltage (J-V) curve of the solar cells was characterized using a solar simulator (Newport, Oriel Class AAA 94063A, 1000 Watt Xenon light source) with a source meter (Keithley 2420) at 100 mW cm⁻² with AM 1.5G irradiation. A calibrated Si-reference cell and meter (Newport, 91150 V, certificated by NREL) was used to calibrate the solar simulator prior to cells measurement. External quantum efficiency (EQE) data were characterized by a solar cell spectral response measurement system (QE-T, Enli Technology, Co Ltd). Temperature-dependent current-voltage (J-V-T) and capacitance-voltage (C-V-T) measurements were

performed using a Solartron Modulab potentiostat equipped with a frequency response analyzer (Ametek Inc).

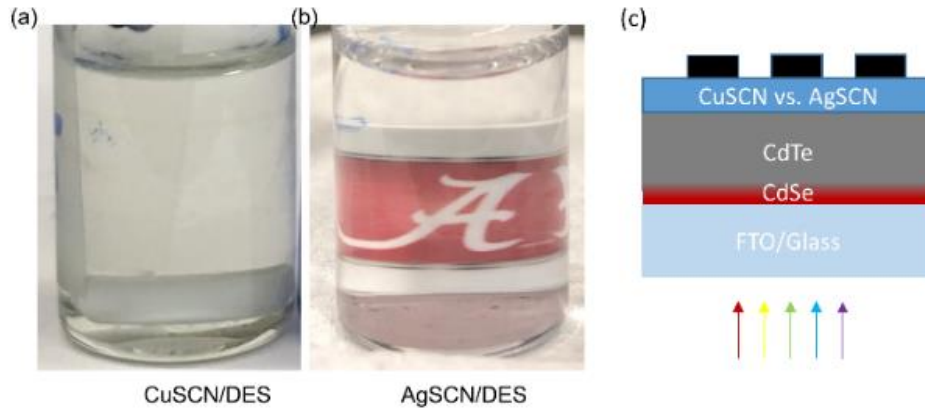


Figure 30: (a) CuSCN and (b) AgSCN solution and (c) CdSe/CdTe heterojunction solar cells with the CuSCN or AgSCN layer as a doping source

The thickness was measured using a Stylus profiler (Dektak II). The back contact for the CdTe solar cells was screen printed graphite without extra Cu source and Ag paste. The finished solar cells were measured using a solar simulator Newport, Oriel Class AAA 94063A, 1000 Watt Xenon light source) with a source meter (Keithley 2420) at 100 mWcm^{-2} AM 1.5G irradiation. A calibrated Si-reference cell and meter (Newport, 91150V, certificated by NREL) was used to calibrate the solar simulator prior to cells measurement. External quantum efficiency (EQE) data were characterized by a solar cell spectral response measurement system (QE-T, Enli Technology, Co. Ltd).

The CdTe film with $\sim 3 \mu\text{m}$ was deposited on the sputtered CdSe ($\sim 100 \text{ nm}$) buffered F-doped SnO_2 (FTO, NSG USA) substrate using the close-space sublimation (CSS) method. The detailed CSS deposition process was reported elsewhere¹²⁵. The CdTe films were thermally treated using the CdCl_2 solution at 400°C for 20 to 30 minutes in the ambient air. The CdTe surface was rinsed using deionized water (DIW) to remove the residual CdCl_2 , following an

etching process using the diluted HCl solution to remove the surface oxides layer before the coating and back contact deposition of AgSCN. For DES-based AgSCN, the solution was denoted as DES-AgSCN, and for DES-based CuSCN, solution was denoted as DES-CuSCN. The thickness of the DES-CuSCN and layers was 30 to 60 nm and the thickness of the DES-AgSCN was 10 to 20 nm, respectively. The thickness was tuned through the spin coater rotation speed. Thicknesses was measured using a Stylus profiler (Dektak II). The back contact for the CdTe cells was screen-printed using graphite and silver (Ag) paste. The cells area is 0.08 cm². The cells were heat treated for about 20 minutes at 200°C to drive the Ag and Cu concentration into the CdTe for increased carrier collection.

4.6 Results

4.6.1 Device performance

The clean transparent color of the solution is in agreement with the previously reported results¹³⁷. CuSCN and AgSCN both have wide bandgaps of >3.5 eV, which also corresponds to its transparency.

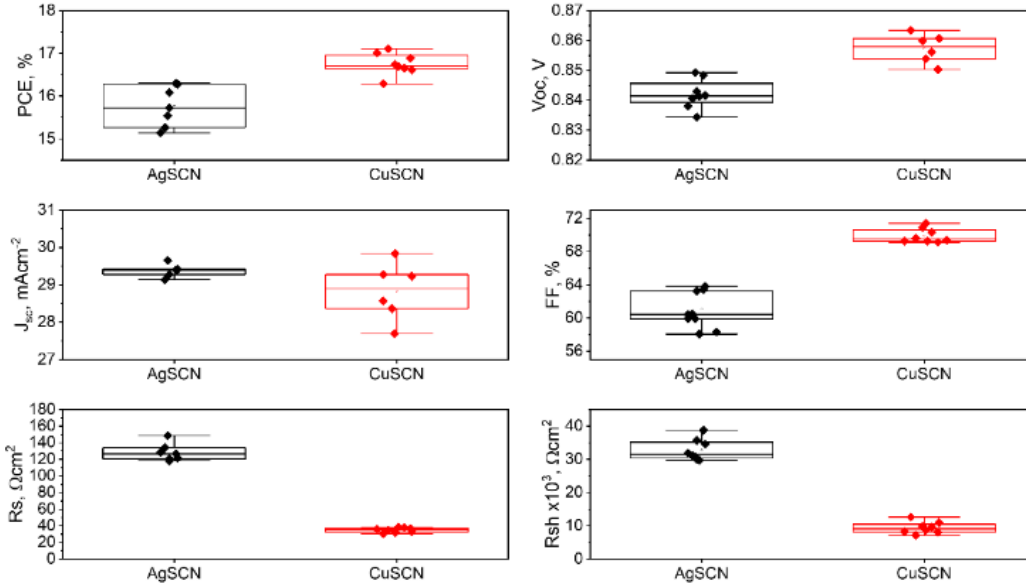


Figure 31: Statistical distribution of (a) PCE, (b) V_{oc} , (c) J_{sc} , (d) FF, (e) R_s , and (f) R_{sh} of CdSe/CdTe solar cells based on solution processed CuSCN and AgSCN layers as doping source

The device structure indicated in Figure 30 a,b shows 10 mg ml^{-1} CuSCN or AgSCN that was spun coated at identical conditions in order to control the dopants concentration and compare the doping effect. Figure 31 shows the statistic distribution of the CdSe/CdTe devices performance with CuSCN and AgSCN, respectively. The CdTe device with CuSCN shows a 1% PCE gain over the cells using AgSCN. The best devices PCE for the CdTe/CuSCN and CdTe/AgSCN can achieve 17.1% and 16.2% respectively. The gain for the CdTe/CuSCN is mostly from the improved V_{oc} and FF, where a 20 mV V_{oc} and 5% FF improvement were observed by using CuSCN as the Cu dopants source. However, the J_{sc} was improved by using the AgSCN as Ag doping source.

4.6.2 I-V and QE on AgSCN using DES

Device performance has shown an increase in J_{sc} of about 29.5 mA/cm^2 using AgSCN as a Ag doping source in comparison to a J_{sc} of 28 mA/cm^2 using CuSCN as doping source. The reduced FF and V_{oc} by employing AgSCN is due to the significantly improved series resistance

compared with that of the CdTe with CuSCN. Interestingly, the shunt resistance of the CdTe with AgSCN was improved about 4 times that of the CdTe with CuSCN. This is probably due to the fact that AgSCN is highly resistive than that of the CuSCN. The average cells performance parameters of CdTe cells using the CuSCN and AgSCN doping source suggests that the Cu doping may be more effective at boosting the device performance with similar dopants concentration, which is in agreement with the previous reported.

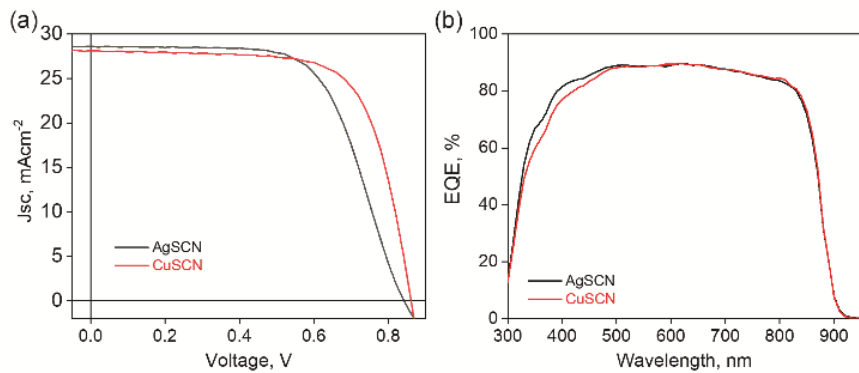


Figure 32: (a) J-V curve and (b) EQE of CdSe/CdTe cells with solution-processed CuSCN and AgSCN

Ag doping effect typically uses evaporation as the preferred deposition technique. However, here our device performance should be better than that of the previous results which may be due to the fine control of the Cu and Ag diffusion. It was reported that CuSCN diffuses slower than that of pure Cu layer on the back of CdTe due to the higher back barrier height of CuSCN/CdTe. Considering that the larger resistivity of AgSCN than that of the CuSCN, we expected that the back barrier height of AgSCN will be more than that of the CuSCN and suggesting a slower diffusion of Ag into the CdTe than that of the Cu diffusion in that of CuSCN. The champion devices with optimization of the CuSCN and AgSCN can reach about 17.15 and 16.2%, respectively.

The current-voltage (J - V) curve, as shown in Figure 32a, suggesting that the CuSCN can improve the V_{oc} and the FF, while the AgSCN can slightly improve the J_{sc} . This observation was associated with the dual role of the CuSCN, i.e., the Cu doping source, and the hole transport layer function. It is known that CuSCN is a cost-effective hole transport layer for several types of solar cells, including the perovskites solar cells. However, there is limited reported for the AgSCN play as a hole transport layer in the solar cells. Thus, it is probably that the AgSCN only plays as an Ag doping source. The electronic transport behavior of AgSCN is out of range of this paper. The EQE spectra of the CuSCN and AgSCN based CdTe devices were presented in Figure 32b. The data confirms that the variation obtained in the J_{sc} of the two doping source is due to the influence of doping type. The Cu doping may diffuse faster than that of the Ag. The excessive Cu in the front junction close to FTO may damage the interface and block the light absorption and then reduce the light absorbed in the CdTe absorber. These phenomena also suggest that AgSCN may improve the long-term stability of CdTe cells, which is a pain point for the reliability issue of Cu doped CdTe.

4.7 Silver (Ag) challenges

It was anticipated that because the atomic radius of Ag is a bit larger than that of Cu, less diffusion would take place which could lead to an increase in device performance. We have found that in comparing CdTe:Ag to CdTe:Cu doping, an increased device performance was seen with that of CdTe:Cu using CuSCN as a Cu doping source.

CHAPTER 5:

GROUP V DOPING IN CdTe SOLAR CELLS

The goal of the work is to develop a process that could further demonstrate an increase in device performance by controlling the doping in CdTe thin film solar cell. By using a cost-effective solution based process that would create conditions for dopant incorporation in CdTe solar cells. Recently, other strategies have been proposed and demonstrated successfully to improve V_{oc} . For example, a higher open circuit voltage (V_{oc}) of above 1.0 V in monocrystalline CdTe with a PCE ~17% by doping with phosphorus (P) has been achieved⁹⁸. However, polycrystalline CdTe devices with 22% PCE suffers a relatively low V_{oc} close to 0.9 V⁸³. It is a huge challenge to introduce P or other group V dopants (eg, As and Sb) into the polycrystalline CdTe to further improve the V_{oc} ¹¹⁵. Group V doping for CdTe is so attractive because theory shows that an increased carrier concentration and stability is possible with Group V doping. In addition to the fact the Group V, has a physical similarity to Te, this makes Group V doping elements an ideal candidate to help promote dopant incorporation and activation in CdTe device¹³⁸. Models and experimental studies have shown that in order to incorporate Group V elements into CdTe, a more aggressive deposition technique may be required^{82, 100, 101, 139-141}. Thus, an alternative way to further improve the V_{oc} using a cost-effective method is applied in this work.

Solution-processed $AsCl_3$ and $SbCl_3$ served as a doping source for CdSe/CdTe thin-film solar devices. Results for both dopants demonstrate a high power conversion efficiency (PCE) of ~ 11%. For decades, mainstream technology has combined fast and simple CdTe deposition

techniques with CdCl₂ activation annealing and Cu doping. Here, the defect chemistry possess strong self-compensation that limits minority carrier concentration and creates a limit for the fill factor, photovoltage and efficiency (PCE%). As and Sb is a promising p-type dopant in CdSe/CdTe solar devices and has demonstrated an acceptable increase in carrier concentration by orders of magnitude higher (10^{16} – 10^{17} cm⁻³) than other dopants without compromising the lifetime of these carriers coupled with high J_{sc} and fill factors. However, uniformity, large-scale production, reproducibility and cost is an issue with standard As and Sb doped CdSe/CdTe devices with high minority carrier concentrations ($>10^{16}$ cm⁻³) with long lifetimes (< few ns). We studied the cost-effective, large-scale, solution-method fabrication of CdSe/CdTe using AsCl₃ and SbCl₃ as the doping sources.

Studies are still unclear about if Group V doping would become an alternative for Group I doping, however; models and experimental results using aggressive facilities have shown a promise in the photovoltaic community about Group V's potential in becoming the successful dopant in CdTe. Upscale fabrication is needed to combat the concern in stability. Group V dopants need to also be able to intergrate easily into an already established value chain to eliminate the concern of complicated manufacturing. Improved manufacturing is needed to further lower all cost associated with the fabrication of devices. More studies need to be done on Group V's ability to become a reliable alternative for converntial doping methods in CdTe.

5.1 Arsenic (As) doping

Using Group V elements to substitute Te vacant site is favorable under Cd rich deposition conditions. Elements like P and As (Group V) are expected to replace Te(Group VI) to form very shallow acceptor states⁷⁵. Unlike the Group I dopants, interstitials are not considered the main compensating defect for group V elements. When a As atom occupies a Te site, it forms a As_{Te}

defect where it is surrounded by four Cd atoms. The As atom (in the Te site) may move toward a neighboring Te atom to form a As-Te bond breaking two bonds with Cd. This results in the formation of a new defect state called the AX center which is a donor defect. AX center defects have lower formation energies making them the main compensating defect for CdTe solar cells. In 2017, T. Ablekim *et al.*, studied defect structures in As-doped CdTe to investigate limiting factors in p-type doping. First principle calculations were also performed and experimental measurements revealed that the activation energy of As is very low and samples have a very low lifetime which indicates a strong compensating defect may be present.

In 2017, T. Ablekim *et al.*, studied defect structures in As-doped CdTe to investigate limiting factors in p-type doping. First principle calculations were also performed and experimental measurements revealed that the activation energy of As is very low and samples have a very low lifetime which indicates a strong compensating defect may be present.

In 2017, A. Nagaoka *et al.*¹⁴² they report the growth of non-doped and As-doped single crystals using the traveling heater method (THM) with a Cd solvent rather than the more common Te solvent. Then in this same year, the same research group Nagaoka *et al.*¹⁴³, studied fundamental defect properties of As-doped Cd-rich CdTe single crystal films and found a dominant As_{Te} was observed and the hallmark self-compensating AX metastability of the As_{Te} center is observed. They also found that quenching could be used to increase the hole concentration in Cd-rich As-doped CdTe films¹⁴³. In 2018¹⁰⁵, they observed a hole concentration of 10^{16} - 10^{17}cm^{-3} range and doping efficiency of 45% for a quenched As-doped single crystal CdTe grown under Cd-rich conditions¹⁰⁵. In this same year, A. Nagaoka *et al.*¹⁴⁴, found that the activation energy is the dominant acceptor in As_{Te} and the AX As_{Te} was observed.

In 2018, E. Colegrove *et al.*¹⁴⁵, determined the diffusion mechanism in both single and polycrystalline CdTe films and found that diffusion is much faster along the grain boundaries for Sb, P and As with a slow bulk diffusion. It is found that As and Sb diffuse primarily through the Te sublattice which suggests that more aggressive conditions are required to incorporate the dopant into the CdTe film¹⁴⁵. In 2018 A. Danielson *et al.*¹⁰³, was able to enhance the conversion efficiency by increasing the doping density higher than achieved with Cu doping while using a CuCl post-deposition heat treatment¹³⁸.

5.2 Antimony (Sb) doping

Antimony (Sb) is a Group V element that acts as a p-type dopant and occupies the Te site forming stable substitutional acceptor defects Sb_{Te} with a low ionization energy of 0.28eV ⁸¹. Sb doping in CdTe can become a challenge, in order to incorporate p-type doping, V_{Te} must form which means that Cd-rich deposition conditions are required. The formation energy of V_{Te} is also lower under Cd-rich deposition conditions which leads to the formation of Sb_{Te} which can become beneficial to the electrical characteristics in two ways. First, due to the conversion of the Cd-rich n-type CdTe to p-type by quenching V_{Te} (shallow donor) with a Sb_{Te} acceptor. Second, Cd-rich films inhibit the formation of lifetime “killing” defects such as Te_{Cd} and Te_i . Both high carrier concentration and high lifetime can be expected for Sb doped CdTe devices.

Incorporation of Sb in the films is the first challenge for dopant incorporation. In order for Sb to contribute to p-type doping by occupying Te sites, it is necessary to create Te-vacancies. This means that Cd-rich deposition conditions are required. Experimental studies show that a series of CdTe films can be deposited with different gas phase stoichiometry and Sb concentrations. Picos *et al.* studied the influence of Sb and the substrate temperature during the growth on the structural, surface roughness, optical and electrical properties of CdTe films¹⁴⁶.

They found that an increased Sb content in the film lead to decreases in the Cd and Te content. For high concentrations of Sb ($\sim 10^{19} \text{cm}^{-3}$) in CdTe, the CdTe becomes an semi-insulating material. At lower concentrations, Sb preferred substituting Te as an acceptor. Huang *et al.* proved the existence of AX centers for the first time¹⁴⁰. J. Santos-Cruz *et al.* studied the influence of the growth parameters of Sb doped CdTe with RF sputtering¹⁴⁷. They found that, with low concentrations the structure is a mixture of zinc blend (ZB) and hexagonal wurtzite (W) phases. Sb atoms in the CdTe lattice favored the stable ZB Phase, and W is considered the metastable crystalline phase. Y. Hatanaka *et al.* attempted excimer (excited dimer) laser assisted Sb doping by diffusion in crystalline CdTe¹⁴⁸. J. P. Nair *et al.* reported in situ Sb doping of polycrystalline CdTe with electrodeposition. PIXE data confirmed the presence of Sb in the film, however no doping data was presented¹⁴⁹. Okamoto *et al.* investigated Sb doping of polycrystalline CdTe deposited by CSS¹⁴¹. Sb doped CdTe powder was used as the source, and improvement of hole density was reported. R.N Bicknell *et al.*¹⁵⁰ showed the first successful growth of p-type CdTe using photo-assisted Molecular Beam Epitaxy (MBE) in which the substrates illumination during the deposition process was found to produce immediate and favorable changes in the electrical properties of CdTe. They obtained a hole concentration of $5 \times 10^{16} \text{cm}^{-3}$ with a mobility of 40-45 cm^2/Vs . An argon laser was used to assist in the chemical reaction and is needed to overcome the potential barriers at the film surface to increase dopant activation. Benson *et al.* observed that enhanced Te-deposition using laser illumination produced more sites for Sb incorporation⁵⁹.

More recently, Clovegrove *et al.* studied the antimony diffusion mechanism in single and polycrystalline CdTe¹⁵¹. SIMS measurements identified fast grain boundary diffusion suggesting that Sb doping may leave the Sb localized around the grain boundaries. This $(\text{Sb}_{\text{Te}})^{-}$ defect could

transition and form an AX center, a donor defect that could form compensation and hinder doping. All of which methods of incorporating Sb into CdTe required aggressive deposition during the processing.

In this study, we applied solution-processed AsCl_3 as hole transport layer (HTL) for the CdSe/CdTe thin-film solar cells using Cl^- solution and compared these results to SbCl_3 as a HTL for CdSe/CdTe thin film solar cells using Cl^- as a solution precursor solvent which could further enhance the incredible properties that Cl has shown in other studies. The improved V_{oc} and FF for the CdSe/CdTe solar cells with the solution-processed AsCl_3 and SbCl_3 lead to 10% and 11% PCE, respectively. The improved device performance benefits from AsCl_3 and SbCl_3 for high V_{oc} and FF, while CdSe window layer accounts for high J_{sc} contributes the efficiency improvements. The cost-effective solution-processed of AsCl_3 and SbCl_3 for CdTe devices provides a promising pathway to reduce the cost of solar energy technology production and other associated cost of manufacturing. The deposition of AsCl_3 and SbCl_3 is shown in Figure 33. The process looks similar but the control of the As and Sb concentrations through careful fabrication and cell architecture was essential in optimizing device performance. To further achieve a higher PCE% of CdTe solar cells, a higher open circuit voltage (V_{oc}) and fill factor (FF) are required.

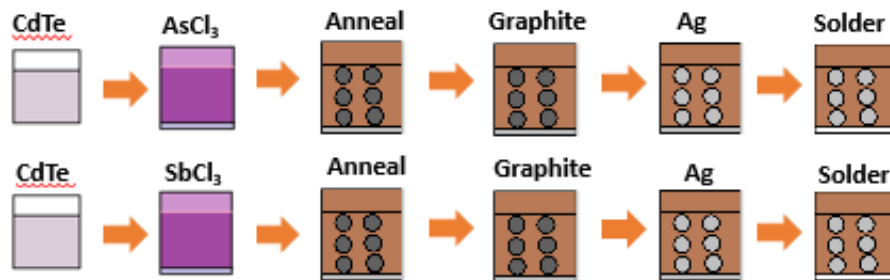


Figure 33: AsCl_3 and SbCl_3 were deposited the same way using diethyl Sulfide (DES) and an aqueous ammonia hydroxide (NH_4OH) solutions were chosen as solvents

Traditionally, to improve the V_{oc} , Cu doping is used as an affordable and effective way to fabricate high efficiency CdTe devices. Recently, other strategies have been proposed and demonstrated successfully to improve V_{oc} . For example, a higher open circuit voltage (V_{oc}) of above 1.0 V in monocrystalline CdTe with a PCE ~17% by doping with phosphorus (P) has been achieved⁹⁸. However, polycrystalline CdTe devices with 22% PCE suffers a relatively low V_{oc} close to 0.9 V⁸³. It is a huge challenge to introduce P or other group V dopants (eg, As and Sb) into the polycrystalline CdTe to further enhance device performance. Group V has been seen in the literature as an appropriate candidate due to its ability to theoretically enhance carrier concentrations in CdTe. In addition to having a similar physical similarity to Te, little work has been done on incorporating Group V elements into CdTe.

5.3 Arsenic (As) and antimony (Sb) doping in CdTe solar cells

The strategy necessary for an improved V_{oc} and PCE of CdTe solar cells when comparing to the sufficient increase in PCE obtained from Cu in previous reports¹⁵², an increased p-type absorber layer is needed to increase the doping of CdTe while also improving the carrier concentration and lifetime. Increasing minority carrier concentrations and lifetimes of these carriers will directly impact the V_{oc} as well as reducing the fatigue of non-ohmic back contacts. Cu has resulted in a significant increase in power conversion efficiency for overall devices^{137, 152}; however, Cu still suffers from the undesirable native defect recombination centers such as Te on Cd antisite (Te_{cd})^{74, 153}. In addition, Cu still suffers from low doping concentrations ($<10^{16} \text{ cm}^{-3}$) and low lifetimes ($>$ few nanoseconds) due to self-compensation by Cu interstitials (Cu_i)^{74, 94, 153}. Unfortunately, limited work has been done to Group V elements such as P, As, Sb or Bi. The work that has been done has shown a difficulty in exceeding hole concentrations of 10^{17} cm^{-3} with a $V_{oc} > 1 \text{ V}$ ¹⁵⁴. It becomes difficult for group V doping to exceed 10^{17} cm^{-3} hole

concentrations while doping levels increases, as doping levels increase this results in a lower power conversion efficiency^{100, 153, 154}.

The source of this doping limitation has not been fully proven but computational models show that this undesired result could originate from the formation of self-compensating AX centers¹⁵⁵. The acceptor type AX center complex compensating behavior happens due to a large lattice relaxation of the substitutional dopant resulting in the conversion to a donor state⁸². There are other possible reasons for low doping activation may be from the self-compensation of Group V interstitials (As and Sb interstitials), solubility limits, formation of competing secondary phases, and compensating or neutral defect complex formation. The understanding of group V doping in CdTe under Cd-rich condition is still developing; the development of processing conditions, hole concentrations, self-compensation mechanism, minority carrier lifetime, and mobility still requires much understanding.

5.3.1 Solvent processed AsCl₃

In this initial study, we applied solution processed AsCl₃ as hole transport layer (HTL) for the CdSe/CdTe thin-film solar with DES and aqueous NH₄OH as solvents, respectively. The improved V_{oc} and FF for the CdSe/CdTe solar cells with the solution processed AsCl₃ lead to 11% PCE with improved series resistivity by AsCl₃ thickness and concentration optimization. The CdSe/CdTe were again grown in collaboration with others by closed-spaced sublimation at a growth temperature of 400- 500° C. With a concentration of 1 to 100 mg/L, and observed increase in power conversion efficiency was obtained.



Figure 34: Solution of AsCl_3 . The concentration is about 1 to 100 mg/L

Figure 34 shows the precursor used during the fabrication of As doped CdSe/CdTe solar devices. The CdSe/CdTe were grown in collaboration with others by closed-spaced sublimation at a growth temperature of 400- 500° C. With a concentration of 1 to 100 mg/L, and observed increase in power conversion efficiency was obtained. So far, we have done the doping of As in CdSe/CdTe devices and now the plan is to fully understand the activation of the As dopants with CdTe devices. More work is to be done on As doping to collaborate with others on further characterizing these devices for future publications.

5.3.2 Device performance

5.3.2.1 I-V curve of AsCl_3 doped CdTe solar cells

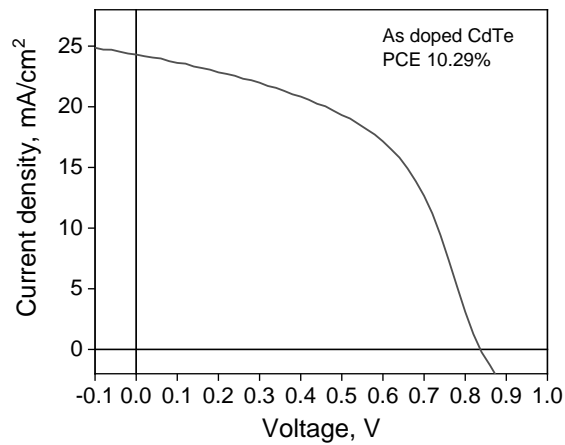


Figure 35: J-V curves of the champion As doped CdTe cells

AsCl₃ doped CdSe/CdTe devices were fabricated via through the solution process, the champion device performance is at about 10.29%, which is lower than the Cu doped CdSe/CdTe devices with a resulting V_{oc} of around 820 mV. These results did not give us as good as a result as the Cu doping in the previous study (PCE 17%) but the As doping in CdTe does give us better results than the undoped CdTe devices. This demonstrates that As could play as the acceptors in the CdTe device.

5.4 CdTe:As device challenges

Even though As is more mobile than Sb, As resulted in a lower PCE% of 10% compared to that of Sb which resulted in a 11% PCE. The challenge for As is that because its ions are small like Cu, they may diffuse too fast into the sub lattice leading to reliability and stability issues that could hinder device performance. In addition, because of the toxic nature of As, university guidelines provided by the environmental, health and safety (EHS) facility at the UA has restricted guidelines to be used to do research with an element like As. Therefore, an extreme careful fabrication process was made with my senior advisor in an effort to use this cost-effective method to enhance the carrier concentration and mobility of carriers in As doped CdTe devices.

5.5 Solvent processed SbCl₃

In this study, we applied solution processed SbCl₃ as hole transport layer (HTL) for the CdSe/CdTe thin-film solar with DES as a solvent. This work is similar to As doping but the improved V_{oc} and FF for the CdSe/CdTe solar cells with the solution processed SbCl₃ has lead to 11% PCE. Results show an improved series resistivity by SbCl₃ thickness and concentration optimization. The CdSe/CdTe were again grown in collaboration with others by closed-spaced sublimation at a growth temperature of 400- 500° C. With a concentration of 1 to 100 mg/L, and observed increase in power conversion efficiency was obtained. So far, we have done the doping

of Sb and As in CdSe/CdTe devices and now the plan is to fully understand the activation of the Sb and As dopants with CdTe devices. More work is to be done on Sb doping to collaborate with others on further characterizing these devices for future publications.

5.5.1 Device performance

5.5.1 I-V curve of SbCl₃ doped CdTe solar cells

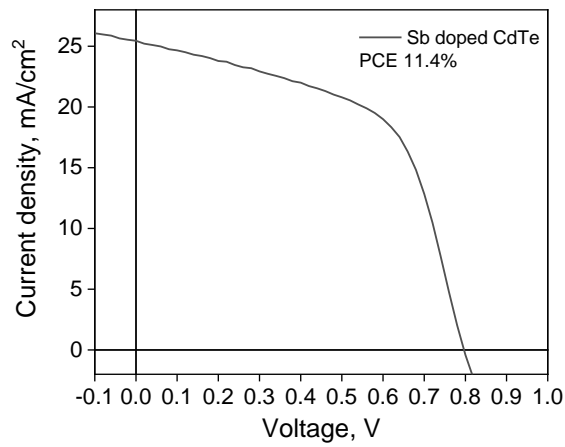


Figure 36: (a) J-V curve of SbCl₃ doped CdTe

SbCl₃ doped CdSe/CdTe devices were fabricated via through the solution process, the champion device performance is at about 11%, which is lower than the Cu doped CdSe/CdTe devices with a resulting V_{oc} of around 800 mV. These results did not give us as good as a result as the Cu doping in the previous study (PCE 17%) but the As doping in CdTe does give us better results than the undoped CdTe devices. This demonstrates that Sb could play as the acceptors in the CdTe device.

5.6 CdTe:Sb device challenges

Sb does exhibit a better dupability than As in addition to having a lower diffusion barrier in CdTe which could lead to dopants being more easily moved throughout the lattice leading to increased lifetimes. Sb is similar to the well studied P dopant in CdTe which further gives

motivation to conduct this cost effect study. Unfortunately, models have shown that Sb is expected to produce a deeper defect than that of As which could lead to recombination centers or even pinning at the fermi level that could hinder carrier transport. In addition, Sb suffers from a low activation energy in comparison to other Group V elements which could lead to compensational effects. The incorporation of Sb with the method of solution processing may yield help non-stoichiometric phases that could enhance grain boundaries that could relate to deep defect states that limit carrier lifetime. Therefore, a more aggressive deposition or more advanced architecture is needed to enhance device performance in CdTe:Sb thin film solar cells.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 Conclusion

This work focused on the fabrication process of Group I and Group V doping in CdTe devices. The device performance was of the main focus during this study and a V_{oc} of 0.857V with a PCE% of 17% was achieved Group I Cu doping using CuSCN as a Cu doping source. In addition, a V_{oc} of 0.842V with a 16% PCE was achieved using Group I Ag doping using AgSCN as a Ag doping source. In our preliminary exploration of Group V doping in CdTe, a PCE of 11% and 10% was achieved using Sb and As doping for CdTe with $SbCl_3$ and $AgCl_3$ as Sb and As doping, respectively. Further studies are needed in an effort to increase the device performance in Group I and Group V doping by means of improving the V_{oc} through an increased carrier concentrations and lifetimes in p-type doping of CdTe solar devices.

6.2 Future work

I plan to continue my study of Group V doping in CdTe with collaborations from others similar to my study on Group I elements in an effort to further understand the mechanism responsible for increasing carrier concentrations and lifetimes of minority carriers in p-type doping of CdTe. Group V doping has not been well established as of today, more study is needed to understand how Group V elements can directly impact the photovoltage properties in CdTe solar cell technologies. Although the current in CdTe solar cells are close to reaching their theoretical efficiency limit, CdTe is still limited by the low carrier concentration and lifetimes associated with low V_{oc} . Refinements and additional device fabrication approaches are needed

to further improve the understanding and performance of CdTe cells. Voltage limitations result from two major sources: 1.) low carrier lifetimes³⁸, typically 1 ns or less and 2.) low carrier density³⁸, typically 10^{14} cm^{-3} .

Advance architectural designs and improved fabrication techniques could allow for an increase in the photovoltage to its theoretical limit of 1.2V. Another major limitation in V_{OC} is the non-ohmic back contact which results from either pinning of the CdTe surface or contact materials lacking the work function needed to match the high electron affinity of CdTe. Here, more study is needed to understand how this non-ohmic contact directly influences electronic behavior. Increased device architecture and further material characterization is needed in order to take CdTe to its ultimate theoretical efficiency limit.

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