SPICE MODELING AND SIMULATION

OF SILICON-CARBIDE

POWER MODULES

by

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A THESIS

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ABSTRACT

The design of power converters relies on computer modeling to accurately predict system electrical and thermal behavior prior to implementation. In the field of wide bandgap semiconductors, the extraordinarily high switching speed of silicon-carbide devices dictates that traditionally inconsequential parasitic elements can impact system level behavior. This is especially true for systems implementing multi-chip power modules. To ensure accurate simulations, a new and precise methodology for modeling these systems is needed.

This thesis formulates a measurement based and empirically-validated methodology for modeling wide bandgap power modules. First, impedance analysis is used to create a parasitic model of the power module's frequency domain behavior. Second, double pulse testing is implemented to characterize the dynamic behavior of the power module. Next, a SPICE model is developed from the frequency and time domain measurements. Finally, the model is validated through its accurate prediction of time domain waveforms and switching losses.

LIST OF ABBEVIATIONS AND SYMBOLS

AWG	American Wire Gauge
CIL	Clamped Inductive Load
DBC	Direct Bonded Copper
DPT	Double Pulse Test
DUT	Device-Under-Test
EPC	Equivalent Parallel Capacitance
ESR	Equivalent Series Resistance
FEA	Finite Element Analysis
FWD	Free-wheeling Diode
GaN	Gallium Nitride
MCPM	Multichip Power Module
PCB	Printed Circuit Board
PEEC	Partial Element Equivalent Circuit
SBD	Schottky Barrier Diode
SiC	Silicon-Carbide
SRF	Self-Resonant Frequency
VNA	Vector Network Analyzer (or Analysis)
WBG	Wide Bandgap
ZA	Impedance Analyzer (or Analysis)

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CHAPTER 1:

INTRODUCTION

In the design of power electronics, silicon-carbide (SiC) power modules promise to enable a new generation of high efficiency, high power systems. Because these systems leverage the fast transition speed of SiC to operate at high switching frequencies, they begin to display near-RF behavior previously not considered by power electronics engineers. These new conditions make mitigating the electromagnetic interference (EMI), preventing system oscillation, and ensuring device longevity more challenging. The complexity of designing power electronics that implement SiC power modules can be reduced with accurate SPICE models. Since SPICE models are not universally supplied by manufacturers, this thesis will establish an empirically validated method for modeling SiC multichip power modules (MCPM) available to application designers.

1.1. Advantages of Wide Bandgap Semiconductors

The field of power electronics has seen exceptional increases in system efficiencies and power density in the last two decades due to the introduction of wide bandgap semiconductors (WBG) [1],[2],[14],[15],[46]-[48],[50]. Silicon-carbide (SiC) and gallium-nitride (GaN) are two mature examples of WBG that have reached the commercial market. In low power, low voltage applications, <500 W and <600 V according to [15], GaN devices offer superior power density and efficiency than SiC because of their typically higher switching speed and typically lower on-resistance [14]. SiC, however, can operate

in medium to high voltage (600 V to 22.5 kV) and high power (greater than 1 MW) applications [15]. SiC also excels in high temperature applications [14]; often with operational ranges above 300℃, compared to the typical limit in Si of 150℃ [1].

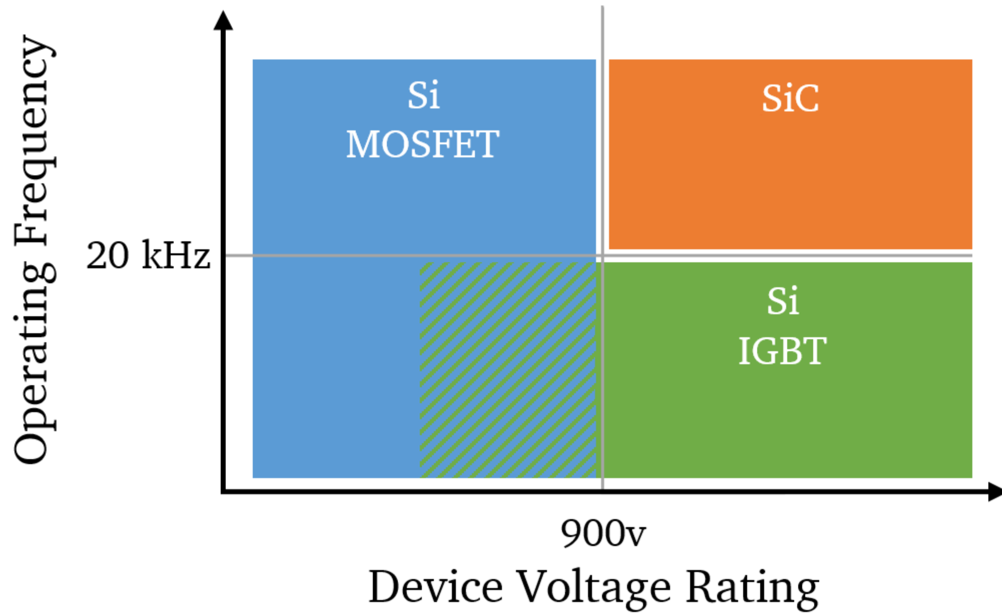

Figure 1: Device Region of Operation [50]

SiC field-effect devices support an operational domain not natively attainable by other Si technologies; Figure 1 shows an overview of the domain suitable to SiC [50]. Like Si IGBTs, they can operate above 900 V, but like Si MOSFETs, they are capable of high switching speeds. Traditionally, higher switching speeds allow for smaller and cheaper filter components [17] in exchange for greater switching losses. Wide-bandgap semiconductors, however, are capable of extremely high dV/dt, enabling higher operational frequencies before switching losses dominate system efficiency. Si IGBTs are rarely operated above 20 kHz [50], but SiC systems have been designed to operate in the range of 100 to 250 kHz with efficiencies greater than 90% [3]. Power electronic systems operating in the range of frequencies supported by IGBT's benefit from the corresponding

assumptions safe for low frequency signals. For example, parasitic inductances on the order of single nano-Henries can be ignored in lower frequency circuits. Because of this, power electronic designers have had little need for the growing set of tools and metrology advancements developed for RF and digital fields, both of which must contend with ultra-high frequency signals. However, as power electronics systems take greater advantage of the near-ideal switching behavior of WBG devices, they face an increasing need for high-frequency design tools and methodologies to be imported into the power electronics community [5].

High switching speed is an important advantage of SiC over Si IGBTs, but the material properties SiC lead to many other device property advantages when compared to Si. For instance, the blocking voltage per unit length of SiC materials is typically an order of magnitude higher than traditional Si materials, and the resulting thinner drift layers lead to substantially lower on resistances in devices [2],[46],[47]. Additionally, SiC is far more reliable and durable than Si [2],[48]. These characteristics contribute to the use of SiC in high voltage and high power converters, systems that require high mean time to failure, and systems that demand high power density. These advantages compensate for the higher cost of SiC in critical applications including military, aerospace, and medical, but SiC also shows promise for many consumer applications such as solar energy [51] and electric vehicles [52].

1.2. The Need for MCPM’s

In the design of devices for power electronics, multichip power modules (MCPM’s) offer many advantages over discrete device packaging. Due to material defects inherent in

semiconductor wafers (which are cut into the die used in discrete parts and power modules), manufacture of both tall die (for higher blocking voltage) and wide die (for higher current capacity) is far more expensive than the manufacture of smaller die. To make high current devices more practical, manufacturers create modules populated with several smaller die. Grouping the die together also leads to more efficient thermal design; it eliminates the need to deal with the individual power dissipation of several discrete parts. High end MCPM's not only use materials with high thermal conductivity, but also account for the thermal expansion of the substrate, reducing strain on the die caused by thermal cycling [53]. Additionally, it is challenging to design parallel arrays of discrete parts with low interconnect parasitics. MCPM's remove this complexity from power electronic system design [18],[53]. MCPM's even assist in EMI containment by grouping the die, a major source of EMI, into a single contained package [5].

Figure 2 shows a simplified circuit diagram of a half bridge MCPM; the diagram ignores parasitic elements and shows only a single MOSFET-diode pair per switch position. Figure 2 also suggests that many MCPM's have discrete diodes embedded in the packaging anti-parallel to the switches. Kelvin terminals (shown as "K" in the figure) are used in both discrete package switches and MCPM's to reduce common source inductance (L_{CSI}), the inductance that couples the power loop to the gate loop.

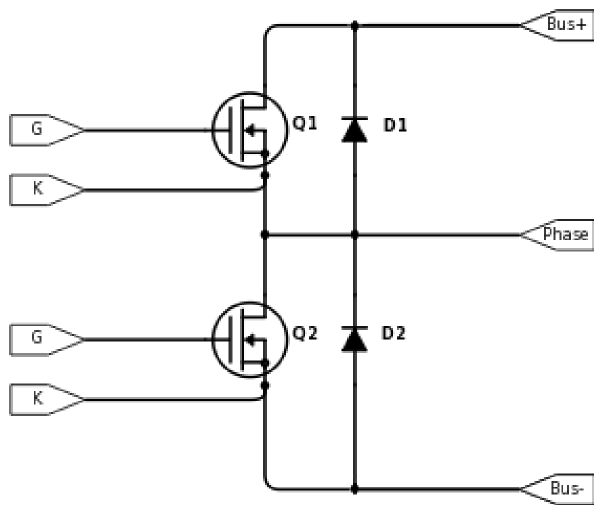

Figure 2: Simplified Half Bridge MCPM Circuit Model

Figure 3 shows a commercially-available half-bridge SiC MCPM manufactured by CREE/Wolfspeed and rated at 1200 V and 120 A. This module is designed to be compatible with the standard 62mm footprint commonly used with IGBT modules, and as such is not optimized for WBG devices.

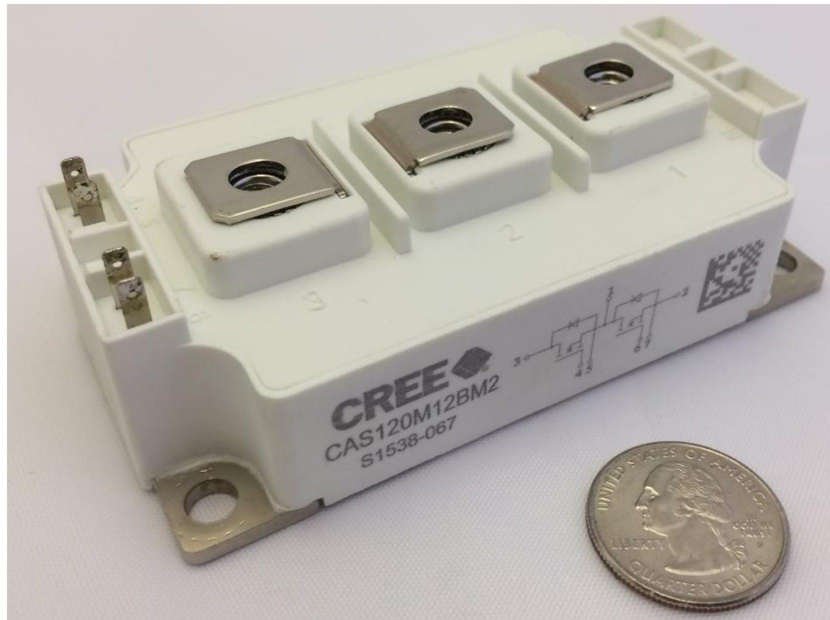

Figure 3: Cree/Wolfspeed MCPM, CAS120M12BM2

Figure 4, on the other hand, presents the HT-2000 packaging that was specifically developed to meet the requirements of WBG die [53]. The HT-2000 implements wide bus-work designed to minimize inductance. Additionally, the low profile of the module results in short distances between the semiconductors and interface, further minimizing parasitic inductance.

Figure 4: HT-2201A MCPM

Although this thesis develops a modeling framework applicable to generic MCPM, a specific device model was developed for the HT-2201A MCPM by Cree/Wolfspeed, shown in Figure 4. The title, HT-2000, specifically refers to the package developed to house a variety of SiC dies in alternate configurations. The HT-2201A contains twelve C2M0080120D SiC die, six at each position due to the half bridge configuration, with six CPW41200S020B SiC Schottkey diodes antiparallel to the die.

1.3. Challenges of WBG Power Modules

Because multichip power modules are populated with multiple WBG die in parallel, they are capable of changes in current even faster than their discrete packaged equivalents

[6]. The authors of [6] also point out that the extreme di/dt's of multichip power modules come with substantial design challenges. They note that 1000 A modules are capable of up to 20 to 50 A/ns, which would cause a 20 to 50 volt drop across 1 nH of inductance in the power loop. While these high edge rates lead to reduced switching losses, they also cause significant challenges in application. For example, small parasitic inductances, considered negligible in the context of slower semiconductors, can contribute substantial underdamped ringing to system response [12] or sustained system oscillation [4]. System ringing that is left unchecked can contribute to switching losses, create additional EMI, and potentially damage or destroy the semiconductor devices [17]. Thus, it is mandatory for both module designers and system designers to minimize parasitic parasitics in high-speed WBG systems. As such, system designers are likely to face unexpected design challenges in initial implementations of SiC MCPM's.

1.4. The Need for Accurate Models of WBG MCPM's

SPICE models of devices, modules, and subsystems can assist system designers in optimization of efficiency, minimization of ringing, and control of EMI. However, poor models can do more harm than good, leading to nonfunctioning prototypes and extended development schedules. SPICE models of WBG devices need to account for packaging inductances to give designers a realistic estimation of the ringing present in the final system [18]. Creating accurate models requires attention to detail; small parasitic inductances must be measured, precise transient tests must be conducted, meticulous tuning must be completed, and finally the system must be empirically validated. Considering these difficulties and the system requirements that demand SiC MCPM's, it

may seem that accurate simulations are prohibitively difficult. In response, this thesis clarifies the process and challenges of modeling SiC MCPM's.

1.5. Organization of Thesis

Considering the foundation this work is predicated on, the distributed work on SiC MCPM modeling can be condensed into a clear and repeatable methodology for creating SPICE models. Chapter 2 examines the work in device modeling documented in the literature, primarily focusing on existing discrete device models, techniques of parasitic extraction, and time-domain analysis of SiC devices. Chapter 3 covers MCPM parasitic extraction (implemented via impedance analysis), and explains the per-terminal impedance model implemented in SPICE. Chapter 4 presents the time-domain testing of the MCPM, detailing the developed test infrastructure and parameters of interest. Chapter 5 demonstrates the process of formulating a model from the empirical results, explaining the development of a model for the semiconductor die, expanding that model to simulate a full MCPM, and tuning the model to the time domain results. Finally, chapter 6 consolidates the conclusions drawn and proposes future work which could improve this methodology.

CHAPTER 2:

LITERATURE REVIEW

The prior chapter attempted to convey both the necessity of simulation models for designers and the difficulties involved in making such models. Fortunately, a substantial amount of work has already been accomplished in the realm of device modeling, and this section explores the foundation upon which this work was conducted and developed.

2.1. MOSFET Device Modeling

Unless provided by the manufacturer, an accurate model of the semiconductor die behavior must be created. Often, discrete part models can be used to simulate each die. Discrete SiC devices have been thoroughly studied, and detailed physics based models of their non-linear behavior have been developed [19],[20]. The authors of [21] point out that [19]'s model is computationally complex in both parameter extraction and simulation; these authors instead opt for the level-1 MOSFET model, a simple and generic model. Despite this, the results of [21] show excellent prediction of time domain behavior, due in no small part to their attention to detail, and their recognition of the importance of packaging parasitics, even in discrete parts.

Unlike the models based on device physics developed in [19],[20], behavioral models are designed with simulation speed in mind. Ignoring the underlying semiconductor physics, they are derived mathematical formulas attempting to only express the correct response for a given input. For example, [22] develops a behavioral model

suitable for very complex simulations that attempts to mitigate some of the inaccuracy traditionally associated with such models. While it was not developed for SiC in particular, it could be adapted for SiC where simulation speed is the priority. Behavioral models have often been considered a good compromise between accuracy and computational complexity [22],[23], and a suitable behavioral model for WBG devices is explored in [24]. Additionally, [23] notes that many WBG models were originally Si models with minor modifications. Many types of die models can be used for WBG MCPM modeling, but the designer should investigate the associated tradeoffs.

2.2. Parasitic Extraction

The discussion of discrete device and die modeling often comes without mention of packaging parasitics; for example, [23] notes that the manufacturer die model under study omitted package parasitics. There is, however, evidence that even in discrete WBG packaging impedances cannot be ignored [25],[26]. As mentioned previously, such problems become even more pronounced in MCPM's [4],[6],[12]. As such, any attempt at modeling power modules without accurate values for parasitic impedances would be incomplete. Die models which do not account for packaging impedances are still useful, however, since extracted parasitics can be appended to die models.

2.2.1. Computational Extraction

One common approach of parasitic extraction is computational modeling, of which there are two main methods. The first is partial element equivalent circuit modeling (PEEC) [31]-[36]. PEEC transforms many small problems in the electromagnetic domain into the circuit domain, allowing a specialized SPICE solver to compute lumped impedance

from the equivalent circuits. Models can be simplified by ignoring inductive, capacitive or resistive effects. Reference [32] notes that PEEC offers the flexibility of time domain or frequency domain solutions and divides modeling into three steps, inductance computation, capacitance computation, and finally network analysis.

The other major simulation method is finite element analysis (FEA) [6],[23],[27]-[30]. FEA is a numerical method that solves the basic physics equations to evaluate interactions at an extremely small level, allowing it to account for many effects ignored by circuit theory. This leads to several benefits of FEA parasitic extraction, as [29] points out. Although FEA can be used in heat transfer, structural analysis, and many other mechanical applications using applicable physics engines, it is applied to parasitic extraction by solving for electromagnetic physics interactions. Authors who use FEA for parasitic extraction have validated their results with impedance analyzers [27],[28] and time domain testing [23], concluding that FEA is a suitable choice for parasitic extraction.

FEA is much more computationally intensive than PEEC for a given problem. Because PEEC transforms EM problems into the circuit domain before solving, it cannot predict physics interactions to the granularity of FEA. FEA is one level of abstraction lower than PEEC, with corresponding increases in both accuracy and difficulty. Because of the affordability of computing power, and FEA's advantage in accuracy, FEA has become more common than PEEC.

Not only are FEA and PEEC capable of predicting self-capacitance and self-inductance, a trait common to all methods, but they also can predict mutual-capacitance and mutual-inductance, the latter of which has a significant impact on common source

inductance [25]. Although the empirical methods avoid the difficulty of developing a complex computer model, one challenge of these methods is the inability to measure mutual inductance; no paper referenced here showed any method to measure the magnetic coupling between the gate-Kelvin loop and power loop.

Many authors note an important drawback of FEA and PEEC; proprietary geometric details and material properties are required for accurate simulation models [18],[37]-[39]. Additionally, neither method can account for tolerance in manufacture, which is easily accomplished in empirical methods by averaging the results of several parts. Finally, FEA struggles to converge on solutions for irregular geometries such as those commonly found in MCPM's [37],[38].

2.2.2. Measurement-Based Methods

Apart from simulation, parasitic extraction can be conducted through direct module measurements. For example, an impedance analyzer (ZA) can be used to measure summed inductances [1],[8],[18],[21],[39],[40], followed by calculating per-terminal impedances [18]. To avoid confusion, papers which used the impedance analyzer mode of a vector network analyzer (VNA) [40], are grouped with those that used a dedicated ZA. Overall the ZA method is the simplest since the impedances are directly obtainable from the raw data [18].

Another empirical method, which requires a VNA, is differentiated because the model is developed using two port scatter parameters. Both [5] and [41] show that S-parameters can be used to make an accurate simulation model of an MCPM. Arguably, using S-parameters for MCPM modeling is slightly trickier than per-terminal impedance

models because two port parameters are more difficult to integrate with die models in SPICE. Otherwise, the method is similar to the ZA method.

One author showed that impedance values can be directly calculated from double pulse testing (DPT) results [42], arguing that the simplicity of the method makes up for the reduced accuracy. Unfortunately, this simplicity comes at an even greater loss of accuracy for MCPM's, as there is no way to differentiate the impact of test stand inductances from module inductances. This is unacceptable for well-designed MCPM's as bus inductance can easily be two orders of magnitude larger than module inductances.

The final empirical method discussed here uses time domain reflectometry, or TDR [37]. This method involves using several algorithms to calculate transmission line models from a set of single-port and two-port measurements. Next, lumped models of the impedances are calculated from the transmission line models. A drawback, as [39] notes, is that TDR suffers from a similar limitation to the simulation methods; internal device geometry and material properties are necessary to create models from measurements. Additionally, [38] points out that TDR is designed to measure structures with a known ground reference, allowing deviations from the characteristic impedance of 50 Ω to be shown. Without a fixed ground reference, measurements based on the transmission line model are of questionable validity. Finally, [38] notes that TDR cannot resolve backplane capacitance as there is no conduction path for the injected signal.

No single method can claim to be the best in all categories; rather, each method has tradeoffs in complexity, accuracy, and time investment. Weighing the advantages and challenges of each method, the technique chosen for MCPM parasitic extraction in this

work is impedance analysis (ZA). Not only is ZA available to the end user without proprietary data, but it also has sufficient accuracy to model the packaging of MPCM with good fidelity. This method has its own challenges, especially in fixture design, but it is less risky and error prone than other methods surveyed.

TABLE 1
OVERVIEW OF MEASUREMENT BASED PARASITIC EXTRACTION

	PROS	CONS
ZA: Per-Terminal Inductance Model	• Simple • Accurate	• Fixture Design
VNA: 2-Port Parameters	• Accurate	• Fixture Design • Difficult implementation in SPICE • Requires multiple measurement configurations (Series and Shunt)
Double Pulse Testing	• Easy	• Inaccurate (unusable for MCPM)
Time Domain Reflectometry	• Impedance behavior can be associated with geometric structures	• Complex • Proprietary Module Details • Unclear fixturing requirements

2.3. Time Domain Evaluation

Time domain testing is a critical step in modeling switching devices, and double pulse testing (DPT) is commonly used to evaluate dynamic performance [3],[7],[21]-[27],[40],[42]-[44]. DPT offers an excellent way to calculate switching losses and system stability of a converter without the difficulties of controller design [43]. Additionally, it isolates the device losses from other frequency dependent losses in the system [25], such as inductor core losses. Establishing a linear trend of measured converter losses across multiple operating frequencies does not accomplish this. Additionally, MCPM's are often implemented in converters rated for 10+ kW output power, and such converters require sophisticated thermal management to handle the necessary dissipation [40]. DPT bypasses

the need for a thermal management system because the test is only conducted for a few microseconds. The brevity of DPT also incurs reduced risk to the device compared to the continuous operation of a converter. Another advantage of DPT is the ability to precisely control the operating conditions such as bus voltage and load current [25]. For these reasons, DPT was chosen over converter implementation to evaluate time domain behavior.

Although DPT offers greater insight into transient device behavior than measuring a complete converter, there remain many concerns for achieving accurate test results. In [44] the authors show that using probes with insufficient bandwidth can artificially reduce the parasitic ringing measured. Converter design guides such as [45] also apply to DPT, so considerations such as minimized gate inductance cannot be ignored. When computing switching losses, precise de-skew technique is critical for accurate measurements [3]. Additionally, [25] discusses the critical nature of bus inductance for high-performance converter design. Bus inductance is often orders of magnitude higher than component inductance and contributes substantially to parasitic ringing. Thus, if bus inductance is not considered in SPICE modeling, there will be poor correlation with time domain results. Finally, special attention must be paid to the placement and design of current shunts, which can greatly increase parasitic bus inductance [6],[44].

Time-domain tests are used in this work for both final tuning of module parameters and validation of the SPICE model. Other authors, however, have used dynamic testing for a larger role in the modeling process. As mentioned before, [42] used double pulse testing entirely on its own for parasitic extraction, though arguably the results include only

an estimation of device impedances. Similarly, [22] used DPT exclusively for the creation of an analytical die model; the omission of device static behavior was justified by the prioritization of simulation speed over accuracy. Another author instead used DPT supplementally to static testing [7]. Many others use DPT for validation of models [21],[23], [24],[40].

CHAPTER 3:

FREQUENCY DOMAIN CHARACTERIZATION

Parasitic extraction of package inductances is an important step in MCPM modeling. Computer simulation such as FEA and PEEC can calculate module packaging inductances, but these methods require proprietary details often unavailable to system designers. In terms of accessibility, impedance analysis is superior. A technique based in measurement, impedance analysis offers sufficient accuracy without proprietary details: only the instrument and module are required.

Measuring the tiny inductances that play critical roles in SiC SPICE simulations requires accurate instrumentation and precise metrology. Even in discrete packages, a few nH of inductance affect system performance [8]. Because MCPM's have far greater current capabilities, even a single nH can influence system behavior. Very few instruments available today are capable of measuring nano-Henry inductances between 10 and 100 MHz. A 1 nH inductor has an impedance magnitude of 60 mΩ at 10 MHz, which is just within the 5% accuracy range of Keysight's E4990a Impedance Analyzer, one of the most accurate impedance analyzers on the market [9]. This value is outside of the rated 10% accuracy range of the Keysight 5061B Vector Network Analyzer [10], another instrument commonly used for parasitic extraction.

Figure 5 shows Keysight's E4990a impedance analyzer configured for measuring an HT-2000 module. This analyzer can measure impedance between 20 Hz and 120 MHz

but is designed to measure discrete parts and printed circuit boards (PCB’s) with RF connectors, not power modules. Creating suitable fixtures to interface MCPM's to the instrument without compromising measurement accuracy is the main challenge of using impedance analysis for module parasitic extraction.

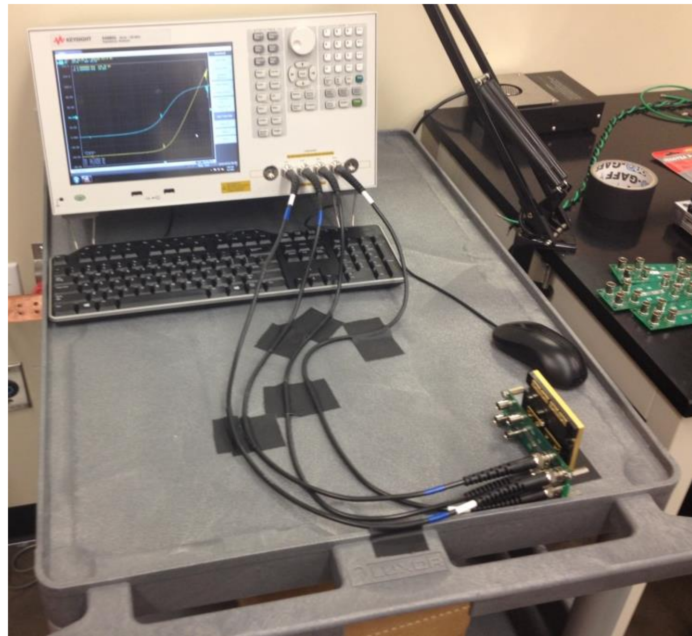

Figure 5: Keysight E4990a impedance analyzer measuring HT-2000 module

3.1. Packaging Impedance of Multichip Power Modules

Performing parasitic extraction requires a general understanding of the basic internal structure of MCPM’s and their packaging inductances. Figure 6 shows an electrical diagram of a generic half bridge MCPM. This diagram accounts for packaging inductances but omits backplane and switch capacitances. Additionally, this diagram shows a single MOSFET and diode in each switch position; whereas a MCPM has many such devices in each switch position.

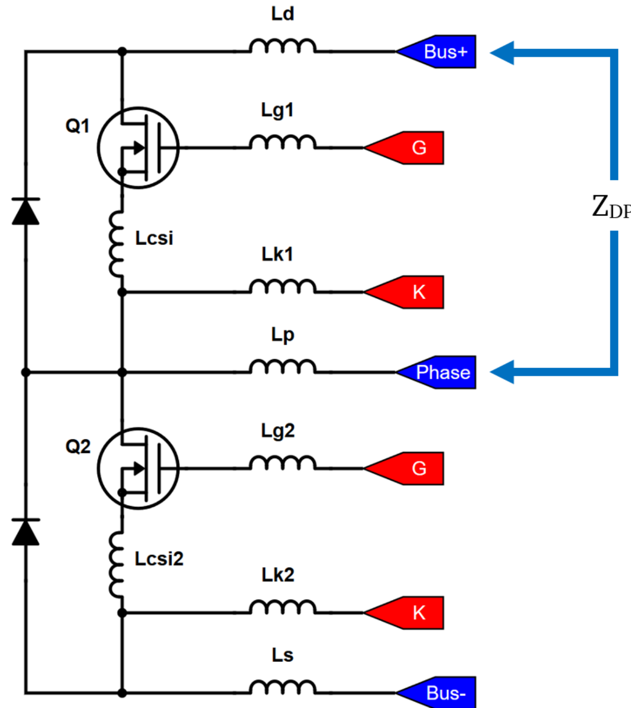

Figure 6: Generic Half Bridge MCPM Circuit Model

To extract the parasitic inductances of such a module, measurements must be taken between each terminal pair. For instance, measuring between the bus+ and phase terminals yields Z_{DP} (the impedance between the drain and source terminals of the top switch). Resolving L_{DP} from Z_{DP} (a process explained in Section 3.6) gives the summation of per-terminal inductances, L_D, L_P, and L_{CSI}. Similarly, any measurement across two terminals of the module will yield a linear combination of per-terminal inductances. A shortcoming of this methodology is no direct method to measure the common source inductance of either switch (L_{CSI}). To compensate, the value of L_{CSI} is initially assumed to be zero and then added to the simulation after time domain analysis. Equation (1) shows the system of impedance equations relating the available terminals measurements to specific per-terminal packaging inductances. Equations (1) through (6) deal with the top switch, and (7) through (12) deal with the bottom switch. Not every possible combination

of terminals must be measured. For example, the impedance between bus+ and Kelvin-2 is not required to solve for the per-terminal inductances. There is a possibility that measuring other combinations could be used to validate impedance measurements, but these measurements would require additional fixtures.

$$L_{DP} = L_D + L_P \tag{1}$$

$$L_{DG1} = L_D + L_{G1} \tag{2}$$

$$L_{DK1} = L_D + L_{K1} \tag{3}$$

$$L_{G1P} = L_{G1} + L_P \tag{4}$$

$$L_{K1P} = L_{K1} + L_P \tag{5}$$

$$L_{GK1} = L_{G1} + L_{K1} \tag{6}$$

$$L_{PS} = L_P + L_S \tag{7}$$

$$L_{PG2} = L_P + L_{G2} \tag{8}$$

$$L_{PK2} = L_P + L_{K2} \tag{9}$$

$$L_{G2S} = L_{G2} + L_S \tag{10}$$

$$L_{K2S} = L_{K2} + L_S \tag{11}$$

$$L_{GK2} = L_{G2} + L_{K2} \tag{12}$$

$$L_{DS} = L_D + L_S \tag{13}$$

3.2. Fixturing

Keysight offers a variety of fixtures that can interface with the E4990a, but none are suitable for measuring packaging impedances of high-performance MCPM's [49]. For instance, Keysight's 16089B fixture, Figure 7 (a), could be used to clip directly to the terminals of a MCPM. However, Keysight specifies that measurements with this fixture are only valid up to 100 kHz, which is insufficient for MCPM's.

Figure 7: Keysight 16089B (a), Keysight 16047a (b)

Figure 8 shows an example impedance measurement, Z_{GK1} of the HT-2000, which is typical of many MCPM impedances. To determine the inductance of this network, the impedance must be measured beyond the self-resonance of the system (in this example, above 10 MHz). Alternatively, a custom wirebond-only module (a MCPM with shorting copper in place of dies) could be used to measure the inductance at a lower frequency, but such modules are rarely available. Thus, the method available to most application designers is evaluation of the production module beyond its self-resonance. Keysight offers a fixture capable of measurements up to 13 MHz, the 16047A of Figure 7 (b); however, it is designed to work with leaded components. Using 3 cm of 18 AWG jumper wire to interface this fixture with power modules would add approximately 24 nH of inductance; in well-designed high frequency MCPM’s, package inductances are typically less than 10 nH per terminal. Thus, the added impedance from the jumper wires would dominate the internal parasitics of a high-performance WBG MCPM, rendering this an unacceptable option.

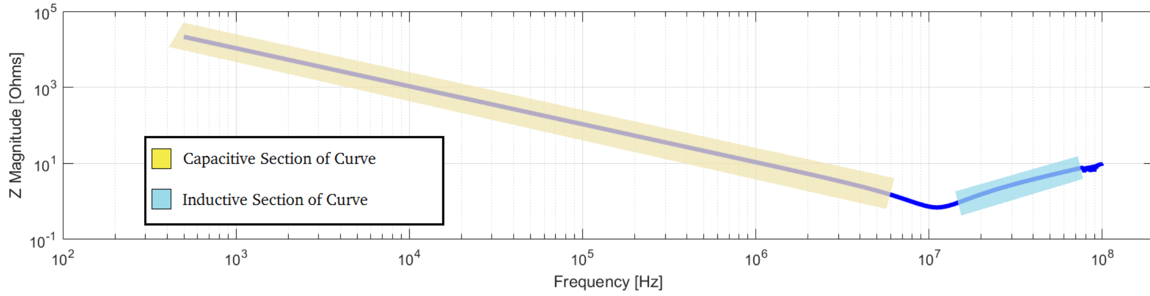

Figure 8: Z_{GK1}'s Impedance Magnitude

Without an adequate interface from the manufacturer, users must develop custom fixtures to accurately measure high-performance modules. The basic goal of power module fixturing is creating low-impedance electrical connections between the terminals of the module and the BNC connectors of the measurement instrument. Figure 9 shows the HT-2000 package; depending on the terminal in question, connections to this module must be made via 6-32 fastener or male header. A logical approach is to develop a PCB with both device connections and BNC terminals. Because of the low impedance magnitude involved in these measurements, four wire measurements are mandatory [11]. Four wire measurements use additional conductors that carry the current necessary to make the measurement and eliminate from the sensing path the voltage drop caused by current through the conductor. Thus, all connections must have a pair of force terminals, through which the stimulus current flows, and a pair of sense terminals, which measure the potential across the device under test (DUT).

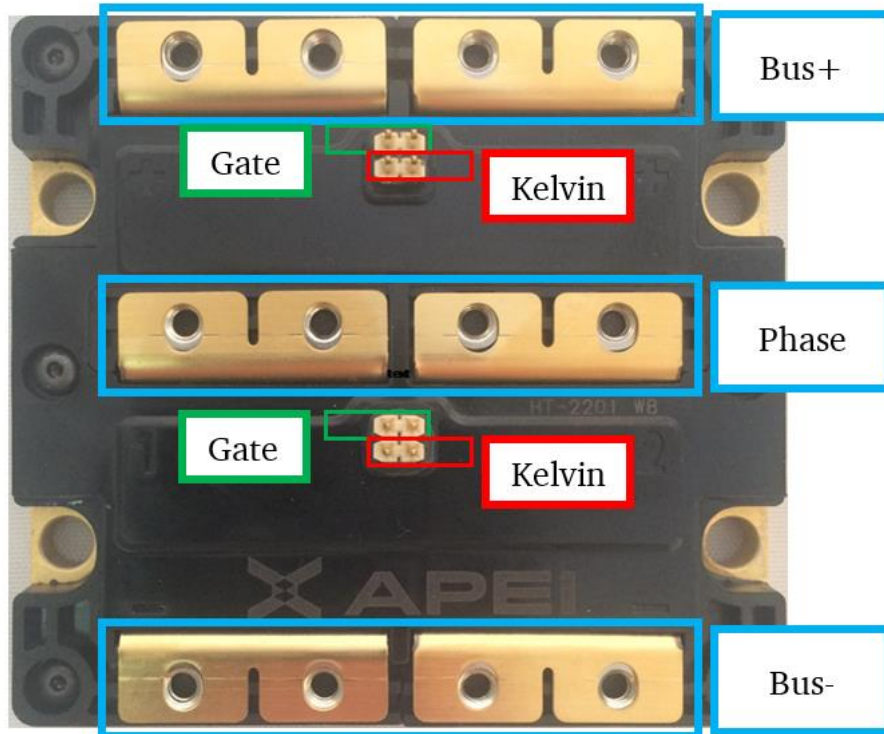

Figure 9: Annotated HT-2000

Figure 10 shows an example of a custom interface PCB designed at UA for measurement of the HT-2000 series modules. This interface board is used to measure the impedance between either of the bus terminals and the phase terminal. It features a pair of BNC connectors to adapt each screw terminal to the impedance analyzer, but ignores the four central pins (the gate and Kelvin terminals). Although the power module studied (HT-2101A) is of half bridge topology, the HT-2000 package can also be populated in a full bridge configuration with four independent switch positions [53]. Thus, the first three adapters developed were designed to be compatible with full bridge variants, which required BNC connectors on both sides.

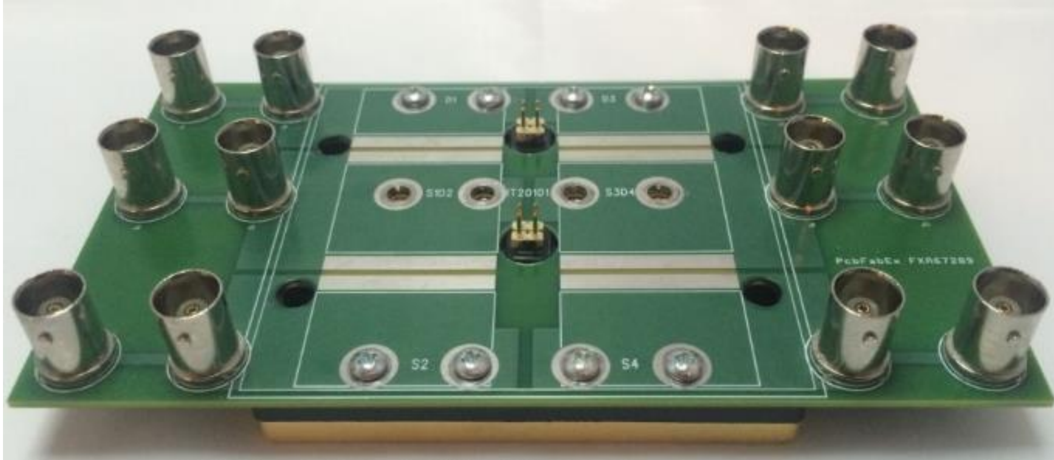

Figure 10: Bus to Phase Interface Board

3.3. Calibration

Due to the requirements of evaluating low-valued impedances, accurately measuring MCPM parasitics requires calibration [11]. The goal of calibration is to compensate for all parasitic elements outside of the DUT, so the calibration must be performed near the terminals of the DUT. Manufacturer supplied calibration kits attach to the end of coaxial cables; thus, they only compensate for parasitic elements in the cables themselves. This calibration process is inadequate for MCPM's because the parasitics of the adapter PCB are ignored and the series inductance of the PCB (potentially greater than the inductance of the MCPM) would be added to MCPM measurements. Instead, calibration must be conducted directly on the interface PCB. A calibration interface in proximity to the terminals under test allows the instrument to compensate for the adapter PCB, rather than measuring it as part of the DUT. Figure 11 shows the adapter PCB from Figure 10, with attention drawn to the exposed copper of the calibration interface.

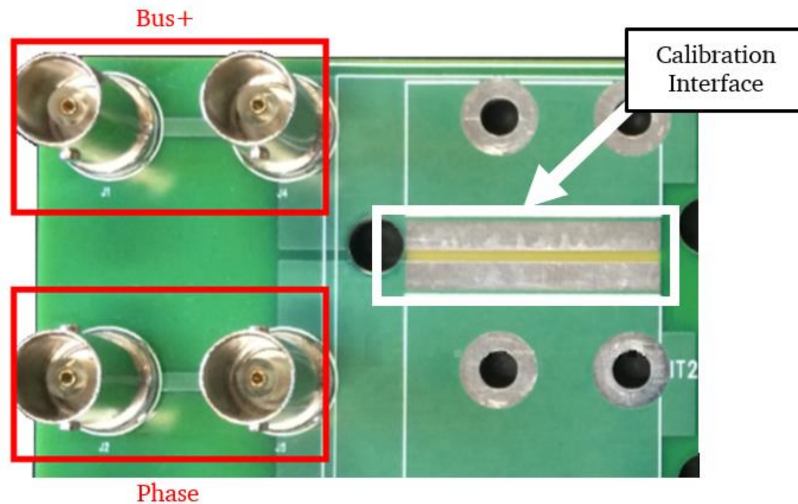

Figure 11: Calibration interface

To calibrate the instrument and associated fixturing, measurements are conducted on open, short, and load standards before the DUT is mounted [11]. First, the exposed copper is left unpopulated to conduct the open circuit test. Next, it is bridged with copper foil for the short circuit test. Minimizing the inductance of the short standard is essential to accurate calibration, so the best practice is to implement a strip of copper foil as wide as the calibration interface. Finally, a 50 Ω resistive load is soldered to the calibration interface for the load test. The load resistor should be nearly ideal within the frequency range analyzed, and using several higher value resistors in parallel (whose combination is 50 Ω) will create an effective load resistor with tighter tolerance and lower parasitic inductance than a single resistor.

3.4. Developed Fixtures

Due to the requirements of fixtures which can measure the parasitics of MCPM above 10 MHz, it is preferable to implement a custom fixture for each measurement, rather than creating a generic fixture for all measurements. Each unique MCPM package also requires new fixtures. For example, four different PCB's were designed to measure the

parasitics elements of the HT-2000. The boards allowed for calibration interfaces directly between each pair of terminals considered during the measurement process.

The fixtures created for the HT-2000 included:

1. Bus to Phase Interface Board
2. Gate to Kelvin Interface Board
3. Gate/Kelvin to Bus/Phase Interface Board
4. Bus+ to Bus- Interface Board

3.4.1. Bus to Phase Interface Board

Figure 12 shows the PCB developed to measure between the bus and phase terminals, along with a schematic representation of the measurement. This board can measure between bus+ and phase (L_{DP}) or between phase and bus- (L_{PS}). To reduce the parasitic capacitance of the fixture, the ground plane (required to connect coax shields) is limited to the edges of the board underneath the BNC connectors. Any surface mounted resistor between the length of a 1206 and a 2512 can fit within the calibration interface.

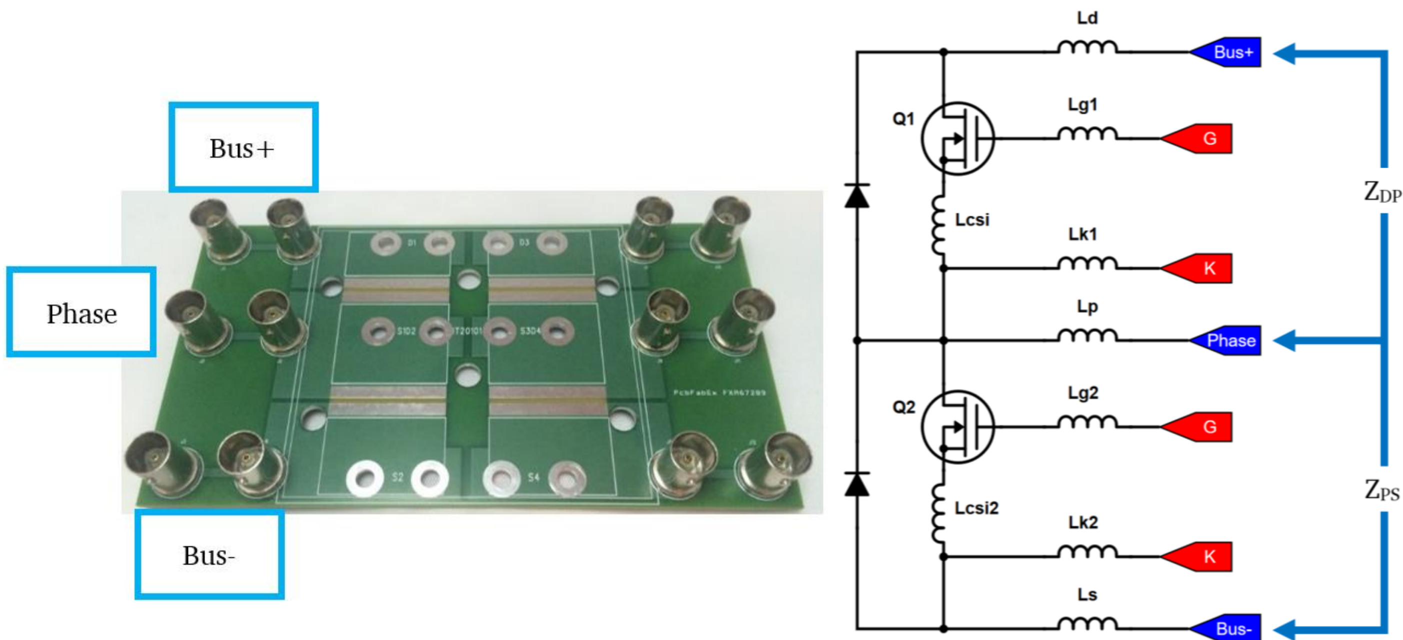

Figure 12: Bus to Phase Interface Board (a), Schematic Representation (b)

3.4.2. Gate to Kelvin Interface Board

The fixture shown in Figure 13 adapts the impedance analyzer to the gate and Kelvin pins of the module. Rather than bolting to the screw terminals, this PCB is soldered to the central pins. Standoffs can be used in the corners to reduce the mechanical stress placed on the device terminals. It is important not to group the BNC terminals too closely together, or the cables will interfere with each other.

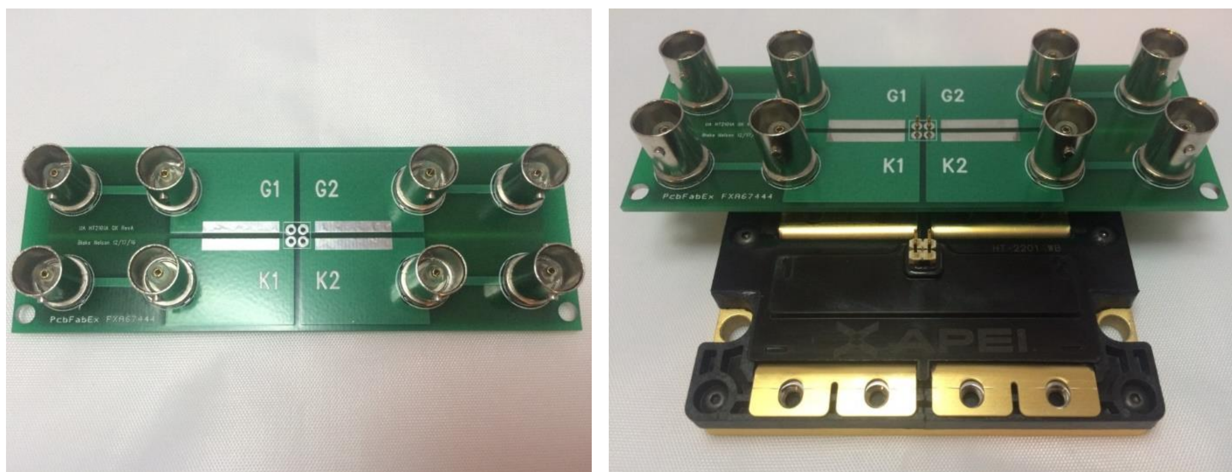

Figure 13: Gate to Kelvin Interface Board (a), mounted (b)

Figure 14 shows a schematic representation of the gate to Kelvin measurement. To measure the bottom switch, the board must be remounted to the lower set of pins, which are structurally identical to the top pins. In this manner, the same board can be used to measure both L_{GK1} and L_{GK2}.

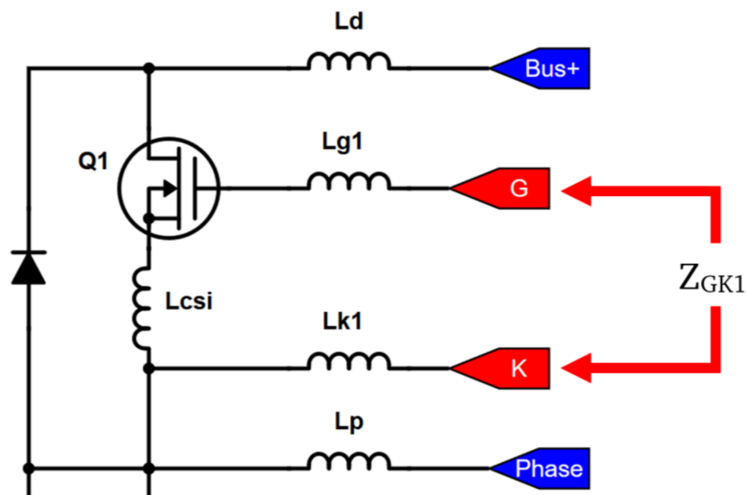

Figure 14: Bus to Phase Interface Board

3.4.3. Gate/Kelvin to Bus/Phase Interface Board

Figure 15 shows the third interface PCB, which is capable of many measurements, each between a terminal denoted in blue and an adjacent terminal denoted in red. The layout of this board allows each calibration interface to be positioned directly between the signal paths of interest. Additionally, the minimum spacing of the BNC terminals requires the traces to fan out from the module terminals. The copper traces are as wide as possible to compensate for this added length. Figure 16 shows all the measurements of which this interface PCB is capable.

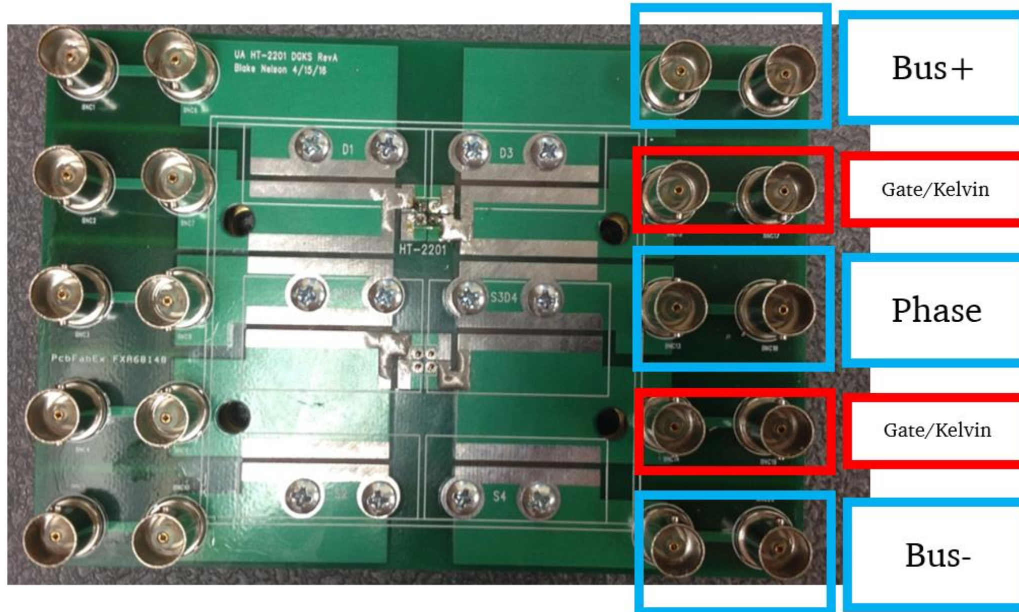

Figure 15: HT-2000 Gate/Kelvin to Drain/Source interface board

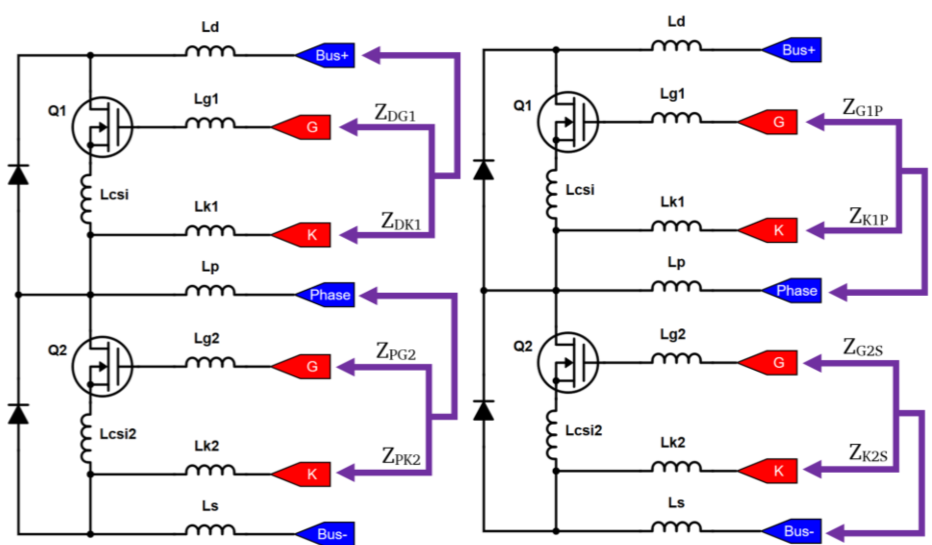

Figure 16: Schematic Representation of Measurement

Figure 17 highlights the method used with this PCB to select the gate or Kelvin terminal for a given switch position. The BNCs with red annotations in Figure 15 can be attached to either the gate or Kelvin terminal using a copper bridge soldered to the board. If gate and Kelvin had separate BNC connectors, there would be no method to calibrate between certain measurements, such as Kelvin and bus+. Alternatively, two unique boards

could be designed, one for gate to bus and the other for Kelvin to bus, but this single fixture can make all gate-loop to power-loop measurements.

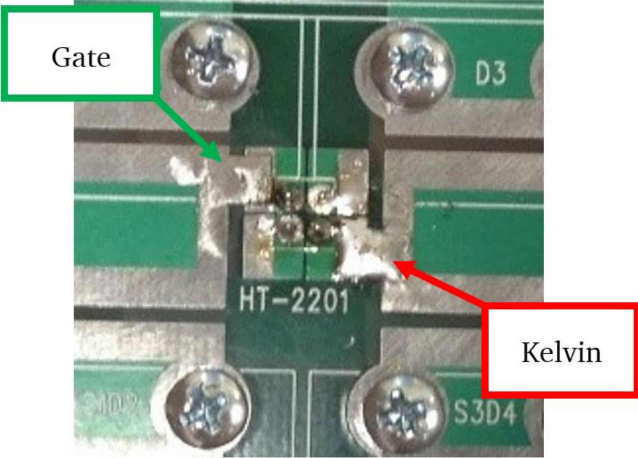

Figure 17: Selection of Gate or Kelvin

3.4.4. Bus+ to Bus- Interface Board

The final interface board is used to measure between the positive and negative bus terminals, or L_{DS}. This measurement is the final unknown needed to fully solve the system of equations (1) through (13). Figure 18 shows the developed interface PCB.

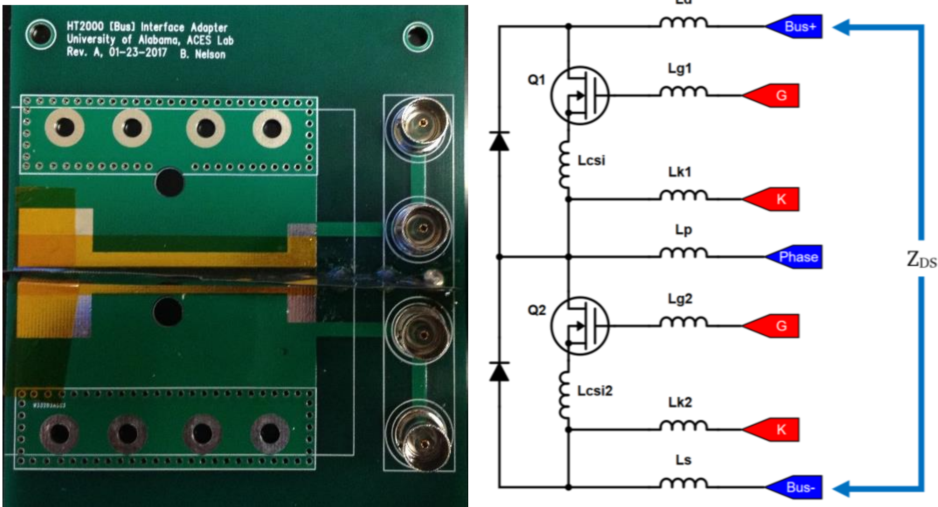

Figure 18: Bus+ to Bus- Interface Board (a), Schematic Representation (b)

Chronologically speaking, the first three boards were developed together, with each improving slightly upon the design of the last. The fourth board, however, was designed

much later and has several alterations from the prior generation. As Figure 18 shows, the board only has BNC terminals on one side of the module. Because of this feature, the board cannot measure full bridge modules. This design decision was made in part because the HT-2000 packaging is being replaced by the recently-introduced HT-3000 module format.

Figure 19: Bus+ to Bus- Interface Board

Another difference of the newer fixture is direct adaptation to the E4990a's front facing ports. Rather than using 1-meter long BNC cables (for example, see the gate to Kelvin board used in Figure 5) this board uses right angle female to female BNC adapters to attach directly to the instrument without any cables. Although the E4990a has compensation profiles for 1-meter cables, omitting the cables entirely ensures the best accuracy at higher frequency (see Section 4.5 of [11]). One concern, however, is that the PCB acts like a lever, applying the module's weight to the sensitive BNC interface of the instrument. Fortunately, the analyzer also has mechanical mounting points near the BNC connectors, which can be used to hold the weight of the module and fixture PCB. The bus+ to bus- board uses tensioned metal brackets to support the module and remove this

mechanical stress from the sensitive interface. Standoffs could also be implemented to protect the instrument.

3.5. Measured Impedances

Because the first three adapters where designed for full bridge compatibility, they offer two sides to take each measurement. Measurements taken with these adapters were repeated on the extra side, inductances were computed from both sets of measurements, and those inductances were averaged. The six measurements of the HT-2000's top switch terminal pairs are shown in Figure 20, and the same six measurements for the bottom switch are shown in Figure 21.

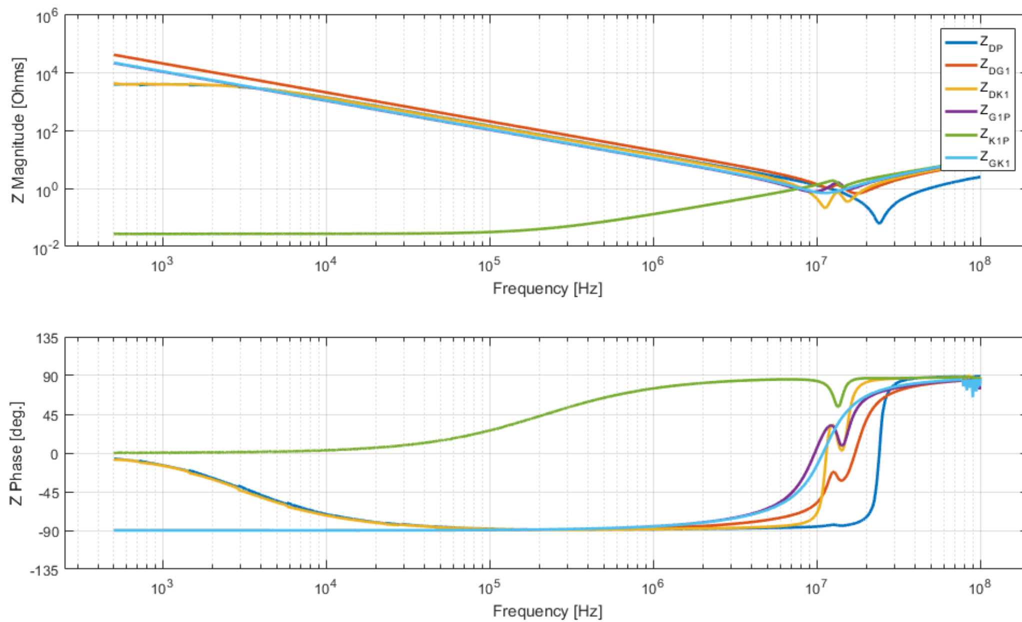

Figure 20: Top Switch Impedance Plots

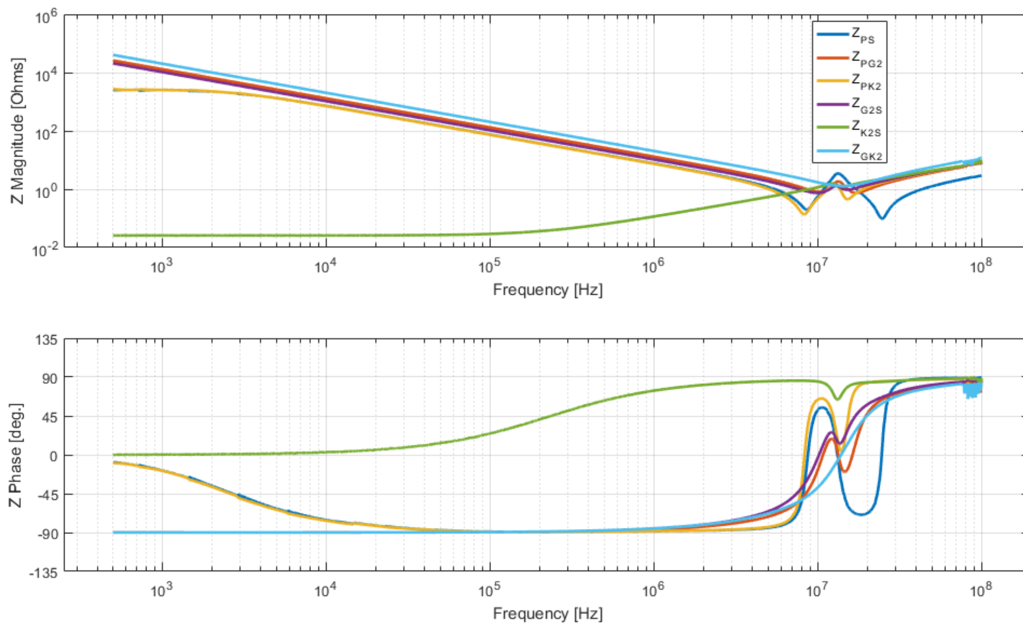

Figure 21: Bottom Switch Impedance Plots

Figure 22 shows a detailed analysis of the gate-Kelvin terminal pair impedance for the top switch, which is representative of all the impedances except Z_{KP} and Z_{KS}. Below 10 MHz, the impedance magnitude falls as frequency increases. This behavior results from the gate to source capacitance of the MOSFET measured in series with the terminal inductances; as is well known, the impedance of a capacitor is inversely proportional to frequency. The self-resonant frequency (SRF) of this terminal pair is approximately 10 MHz, at which point, the magnitude trend changes. Above the SRF, the impedance contributed by the capacitor no longer makes a substantial contribution to the overall impedance. Instead, the rising impedance of the series inductance dominates. For this reason, calculation of packaging inductances requires measurement beyond the SRF (or a wirebond module). These factors indicate that Z_{GK1} can be accurately modeled with a series RLC circuit.

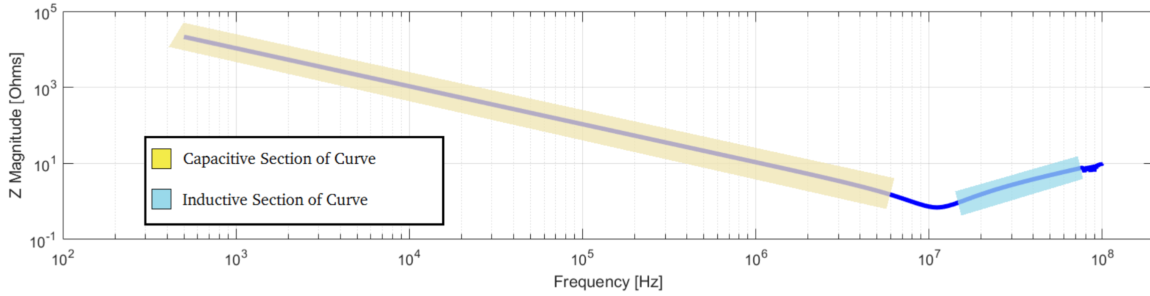

Figure 22: Z_{GK1}, Capacitive-Inductive (CL) Response

Figure 23 provides a detailed analysis of the Kelvin-source terminal pair impedance for the top switch of the module under consideration. Because the Kelvin and source terminals of switching devices are electrically connected with no interposed semiconductor element, the impedance between them is effectively a lossy inductor. The magnitude's independence from frequency below 100 kHz is characteristic of a resistor, and beyond that frequency the magnitude shows the frequency-dependence expected for an inductor. Therefore, it is reasonable to expect that Z_{K1P} can be modeled with a series RL circuit.

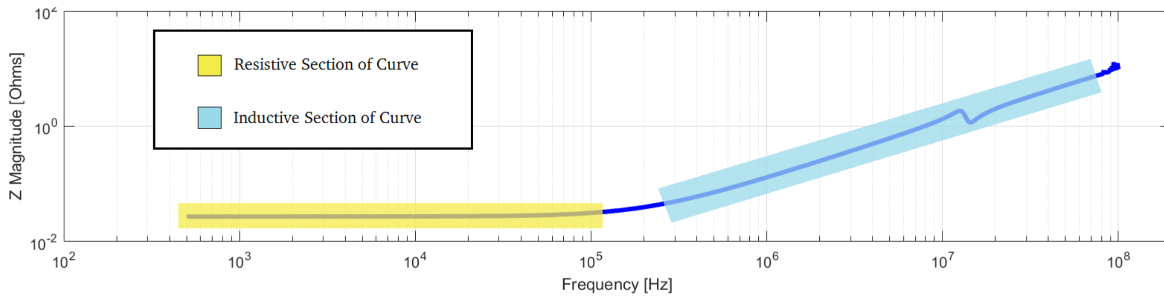

Figure 23: Z_{K1P}, Resistive-Inductive (RL) Response

3.6. MATLAB Analysis and Results

In this work, custom-designed MATLAB scripts are used to compute inductances by fitting a parasitic model to the raw impedance data measured with the ZA. The model's impedance is then visually compared to the graphed data to evaluate the quality of the fit. The outcome of this process for the drain-phase impedance (Z_{DP}) for the module under consideration is shown in Figure 24. In this case, the deviation below 3 kHz indicates the

series RLC model cannot account for all features of the device. The goal of the model, however, is to predict the parasitic inductance of the module, which primarily affects the behavior above resonance. From 25 MHz to 100 MHz, the model prediction is accurate.

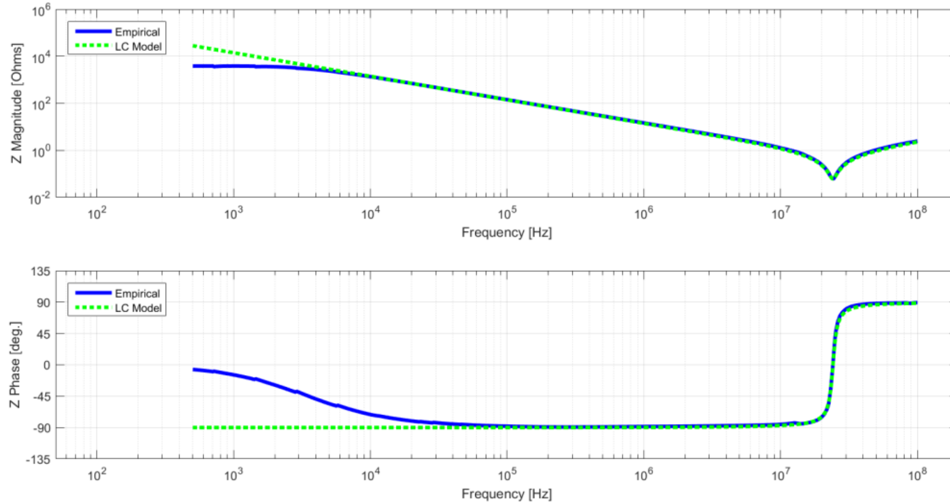

Figure 24: Z_{DP} VS. LC Model

Although MATLAB was used to create a complete model of the measured impedance, this is not strictly necessary. The modeling script could calculate inductance directly, using only the data beyond self-resonance. However, the small frequency range in which inductance can be calculated makes fitting the model challenging for a well-designed (low-inductance) MCPM. Additionally, instrument error increases with frequency, so the uncertainty of the inductance estimates would be greater. Instead, the inductance is calculated though an estimate of the capacitance and SRF. First, capacitance is calculated using a least squares fit across the capacitive region, which is below the SRF. Next, the resonant frequency is estimated using the minimum point of the magnitude data. Finally, the series inductance is estimated with Equation (15). This method of calculating inductance results from rearranging Equation (14), the expression for ω_0, which is the

natural (resonant) frequency of a second-order RLC network. An added benefit of computing the full model is error checking; a total model gives visual confirmation of the inductance estimate accuracy.

$$\omega_0 = \frac{1}{\sqrt{LC}} \quad [67] \qquad (14)$$

$$L = \frac{1}{C * {\omega_0}^2} \qquad (15)$$

TABLE 2
GROUPED PACKAGING INDUCTANCES OF HT-2000

L_{DP}	L_{DG1}	L_{DK1}	L_{G1P}	L_{K1P}	L_{GK1}	
3.99	10.37	16.83	18.40	19.15	13.73	L_{DS}
L_{PS}	L_{PG2}	L_{PK2}	L_{G2S}	L_{K2S}	L_{GK2}	6.37
1.99	7.05	17.38	16.66	17.05	15.40	

*All Values are in nH

The inductance values estimated from the raw measurements shown in Table 2 are grouped inductances. For example, the inductive portion of Z_{DP} represents the series combination of L_D and L_P as described in Equation (1). Therefore, after computing a grouped inductance value for each raw measured impedance, the linear system of equations must be solved to find device impedances linked to the desired equivalent circuit model. A simple way to solve such systems is in matrix form. Equation (16) shows the "A*x=b" matrix form of the system. Since the estimated inductance in Table 2 will contain some error, a solution to this system of equations does not exist; instead, numeric approximation is required to estimate a solution. Both least squares approximation and Moore-Penrose pseudo-inverse were used to estimate solutions for the HT-2000 module, but in all cases, the results from these two approximation techniques were identical to several decimal places.

$$
\begin{bmatrix}
1 & 0 & 0 & 1 & 0 & 0 & 0 \\
1 & 1 & 0 & 0 & 0 & 0 & 0 \\
1 & 0 & 1 & 0 & 0 & 0 & 0 \\
0 & 1 & 0 & 1 & 0 & 0 & 0 \\
0 & 0 & 1 & 1 & 0 & 0 & 0 \\
0 & 1 & 1 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 0 & 1 \\
0 & 0 & 0 & 1 & 1 & 0 & 0 \\
0 & 0 & 0 & 1 & 0 & 1 & 0 \\
0 & 0 & 0 & 0 & 1 & 0 & 1 \\
0 & 0 & 0 & 0 & 0 & 1 & 1 \\
0 & 0 & 0 & 0 & 1 & 1 & 0 \\
1 & 0 & 0 & 0 & 0 & 0 & 1
\end{bmatrix}
\begin{bmatrix}
L_D \\ L_{G1} \\ L_{K1} \\ L_P \\ L_{G2} \\ L_{K2} \\ L_S
\end{bmatrix}
=
\begin{bmatrix}
L_{DP} \\ L_{DG1} \\ L_{DK1} \\ L_{G1P} \\ L_{K1P} \\ L_{GK1} \\ L_{PS} \\ L_{PG2} \\ L_{PK2} \\ L_{G2S} \\ L_{K2S} \\ L_{GK2} \\ L_{DS}
\end{bmatrix}
\quad (16)
$$

Table 3 shows the final extracted per-terminal per-terminal inductance estimates for the HT-2000 module. These values correspond with the parameter names shown for the module equivalent circuit in Figure 6. The bus inductances (L_D, L_P, and L_S) are lower than the gate and Kelvin inductances. This result is expected due to the wide copper interconnects required to support the module's current rating.

TABLE 3
COMPILED PACKAGING INDUCTANCES OF HT-2000

L_D	L_{G1}	L_{K1}	L_P	L_{G2}	L_{K2}	L_S
2.32	8.18	11.79	3.85	6.36	11.72	4.45

*All Values are in nH

3.7. Error Analysis and Approximation

Table 3 introduces the per-terminal inductances of the HT-2000 as specific numeric values. However, assuming the values are perfectly accurate is unrealistic, and the uncertainty associated with these values can be estimated. This requires several sequential steps: (a) determining the error of the raw data, (b) propagating the error through the

inductance curve-fitting procedure, and (c) propagating the error from the grouped inductances to the final per-terminal inductances.

First, the error intrinsic to the measurements must be quantified. This error is introduced from both the instrument itself and the fixturing [11]. The datasheet of the E4990a [9] offers a straightforward formula to compute the percent error from the measurement settings, measured impedance value, and frequency of the stimulus waveform. Equation (17) shows the error formula applicable to both the instrument and fixtures. When evaluating instrument error, each element (proportional error, short repeatability, and open repeatability) can be calculated from the conditions of the test.

$$E = E_P + \left(\frac{Z_S}{|Z_X|} + Y_O * |Z_x| \right) * 100 \qquad (17)$$

E : Error [%]

E_P : Proportional Error [%]

Y_O : Open Repeatability [S]

Z_S : Short Repeatability [Ω]

Z_X : Magnitude of Impedance Under Test [Ω]

The second, and more challenging, part of determining the error of the measurements is estimating the error introduced by the custom fixture. For Keysight OEM fixtures, values for each element are provided in the data sheet [58]; Keysight recommends that users rely on these values for calculation of fixture error [11]. For the custom fixtures, a method to estimate fixture error was required. The repeatability of open and short calibration represents the residual parasitics which cannot be perfectly calibrated out of

the fixture. Both values were estimated by calibrating the fixture and repeatedly measuring the residual of the short and open standard; [11] recommends 50 measurements.

The proportional error Keysight specifies is a percent error independent of DUT magnitude but dependent on frequency. Proportional error can be estimated from the variance of a statistically significant number of measurements, which requires a carefully selected standard to ensure other forms of error do not significantly contribute to the proportional error. A precision 1 kΩ resistor (Caddock MP915) was chosen to test proportional error; not only is it large enough for short repeatability to be negligible and small enough for open repeatability to be negligible, but 1 kΩ is also in the range of the E4990a's peak accuracy. Figure 25 shows the estimated proportional error of the custom fixture in blue. The tested precision load resistor showed characteristics of parasitic capacitance at high frequency, but with no instrument more accurate than the E4490a to evaluate the standard, the trend was assumed to be proportional error. Equation (18) is the model developed to predict proportional error, plotted in black on Figure 25. This model was fit to be greater than the measured error across all frequency.

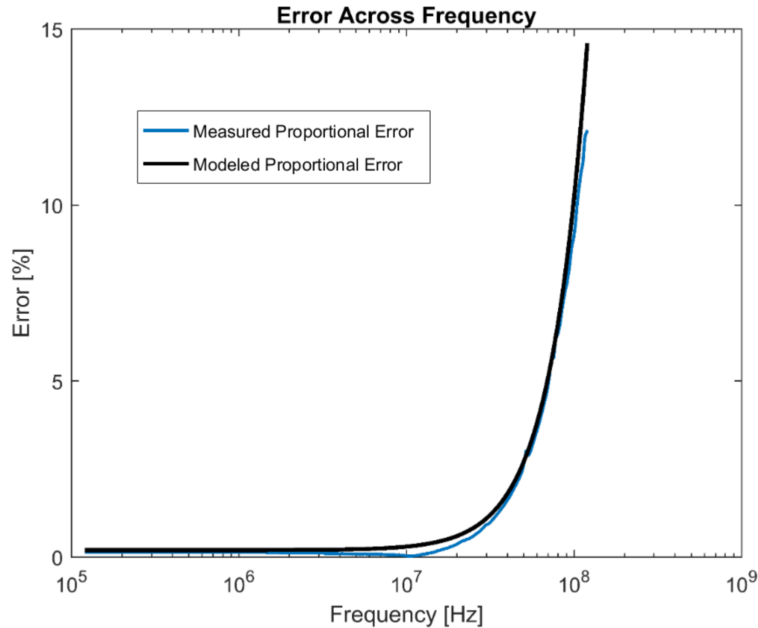

Figure 25: Estimation of Proportional Error for the Bus+ to Bus- Fixture

$$E_P \; = \; .2 \; + \; 10^{-15} * f^2 \qquad [\%] \tag{18}$$

Additionally, no attempt was made to remove instrument error from the estimations of fixturing error, but both are summed to compute total measurement error. Thus, the instrument's error is double counted. Figure 26 demonstrates the measured impedance of the Bus+ to Bus- measurement for the module under consideration, overlaid with error bars representing the total measurement uncertainty. The error is calculated at each frequency measured, but for clarity, the error bars are only plotted at discrete frequencies; plotting them at the hundreds of sampled frequencies renders the plot unreadable. This example result show the total measurement uncertainty for the cableless fixture (Figure 18), but these techniques can be used to create error estimates for any ZA results; a similar range of error is expected of the other fixtures. The approximation for the uncertainty in Figure 26 peaks at 16.3% error at 120 MHz. Because the higher frequency data is not

used to predict inductance, this large error above 30 MHz does not significantly degrade the extracted inductances.

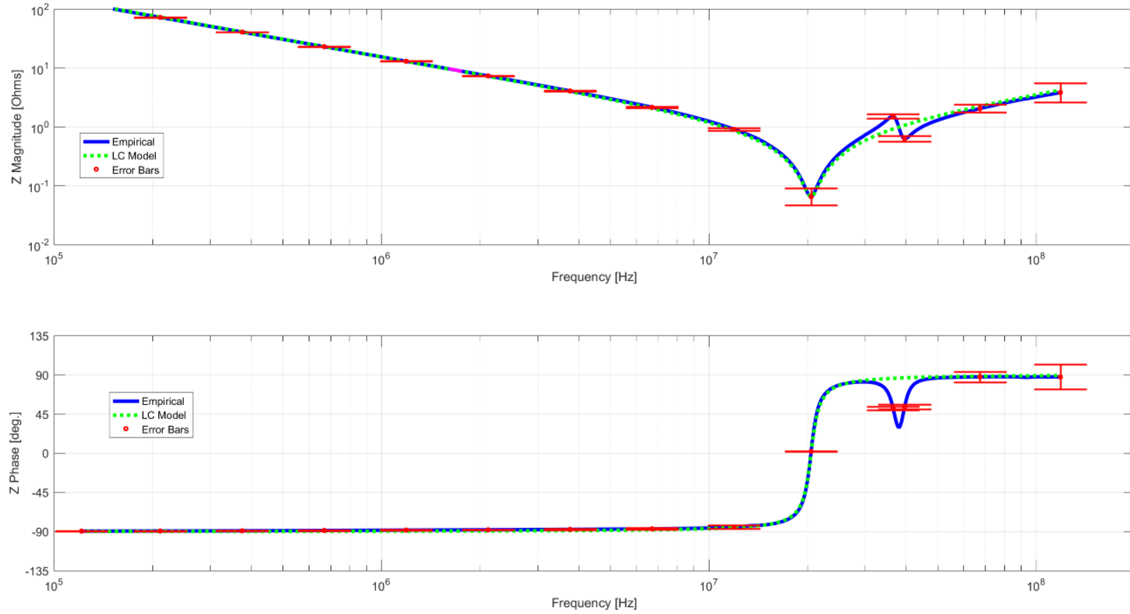

Figure 26: Bus+ to Bus- Measurement and Error Bars

The error bars overlaid on the magnitude plot of Figure 26 require special attention to plot correctly on the log scale shown. Reference [59] states that correct error bars on plots with logarithmic y-axis should be symmetric about the primary data point. To do so requires recognizing that the function being plotted is actually log(y), where y is the test data and δy is the absolute uncertainty. Directly plotting the error as log(y±δy) will result in asymmetric bars with longer bottom sides. If the plotted data is considered a new variable z = log(y), then the error bars span z±δz. In [60], the error propagation of δz in terms of δy is shown to be δz = δy/y for z = log(y); δy/y is the relative error of the variable y. Unfortunately, solving for δz is not sufficient to plot the error bars since δy is the input used by MATLAB's errorbar function. Therefore, equation (19) must be solved for δy to

find the correct input for the error bar function. Equation (23) shows the solutions for the upper and lower error bar inputs.

$$\log(y \pm \delta y) = z \pm \delta z \tag{19}$$

$$y \pm \delta y = 10^{z \pm \delta z} \tag{20}$$

$$y \pm \delta y = 10^{\log(y)} * 10^{\pm \delta z} \tag{21}$$

$$\pm \delta y = y * 10^{\pm \delta z} - y \tag{22}$$

$$\delta y = \pm y * (10^{\pm \delta z} - 1) \tag{23}$$

With the uncertainty of the experimental data known, the uncertainty of the inductance curve-fit procedure can be calculated. Because inductance is calculated by the inverse of capacitance times resonant frequency squared, the uncertainty of capacitance estimate and the resonant frequency estimate are first required. A worst-case approximation of uncertainty in the capacitance estimate can be found using the minimum and maximum capacitance possible for the error. Since capacitance is estimated from the slope of the impedance magnitude within some user-specified frequency bounds, each of these two extremes can be calculated by adding or subtracting the maximum error at the edges of this window. This process assumes the slope is fit using only two points with maximum error at each point, but the slope is estimated via a least squares curve fit incorporating all available data within this window. It is reasonable to assume the accuracy of the actual estimate should be better than this approximation of uncertainty. To estimate uncertainty in the resonant frequency estimate, the measurements before and after frequency of minimum impedance are assumed to be the bounds within which the

resonance must reside. Measuring more points near resonance with the ZA would give a better approximation of resonant frequency and further reduce the curve-fit uncertainty.

In [60], Baird explains that a conservative approach to propagate uncertainty for an equation of two variables is to assume that the deviations in the two variables add such that the resulting value lies as far from the central value as possible. Using this approach, the maximum and minimum values for the grouped inductances (Table 3) were computed based on worst case uncertainty in both the capacitance and resonant frequency estimates. These methods estimate L_{DS} as 5.7 ±.15 nH based on the data from Figure 26. Because each per-terminal inductance is a linear combination of the measured inductances, the final estimated uncertainty for the results is ±.3 nH.

TABLE 4
UNCERTAINTY OF PACKAGING INDUCTANCES

	L_D	L_{G1}	L_{K1}	L_P	L_{G2}	L_{K2}	L_S
Min	2.02	7.88	11.49	3.55	6.06	11.42	4.15
Max	2.62	8.48	12.09	4.15	6.66	12.02	4.75

*All Values are in nH

CHAPTER 4:

TIME DOMAIN CHARACTERIZATION

The next step in the MCPM modeling procedure is dynamic characterization. Rather than evaluating the MCPM by building a power electronics converter, double pulse testing is (DPT) conducted. DPT simulates the operation of a hard-switched converter and is used to evaluate device dynamics, switching losses, and edge rates. The DPT procedure enables the behavior of both switching events (on and off) to be measured at a specific operating condition, defined by the load current and bus voltage. Figure 27 shows a simplified schematic of a DPT test stand, which requires a high voltage supply, a large capacitor bank, gate drive circuitry, a load inductor, and the power module under test. In this configuration, only the bottom switch, Q_2, is switched and measured; Q_1 is held off by the top gate drive. The anti-parallel diode of Q_1, however, is essential to the test. This diode functions as the freewheeling diode, giving the current of the load inductor a path to circulate when Q_2 is turned off, thereby clamping the inductor. For this reason, DPT is also referred to as clamped-inductive-load (CIL) testing.

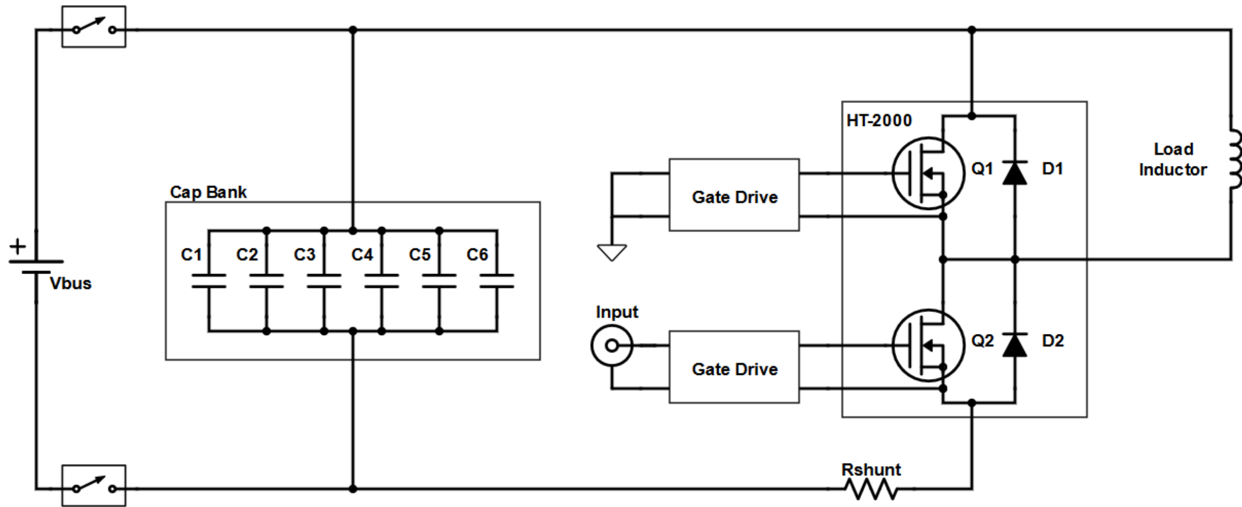

Figure 27: Schematic of Double Pulse Test

The values of gate to source voltage (V_G), drain to source voltage (V_{DS}), drain current (I_D), and inductor current (I_L) are measured during DPT (depicted in Figure 28). Monitoring V_G on the oscilloscope gives an excellent signal for triggering, a clearer indication of the starting and ending of transition events, and a frame of reference for the results. Measuring V_{DS} is not only necessary for calculating switching losses, but also monitors the voltage induced stress applied to the module during switching events and parasitic-induced ringing. I_D is the other factor needed to calculate switching losses and is helpful in identifying shoot through current if the top switch closes due to a spurious gate signal. Because I_D rings during testing, measuring I_L gives a clearer indication of current set point.

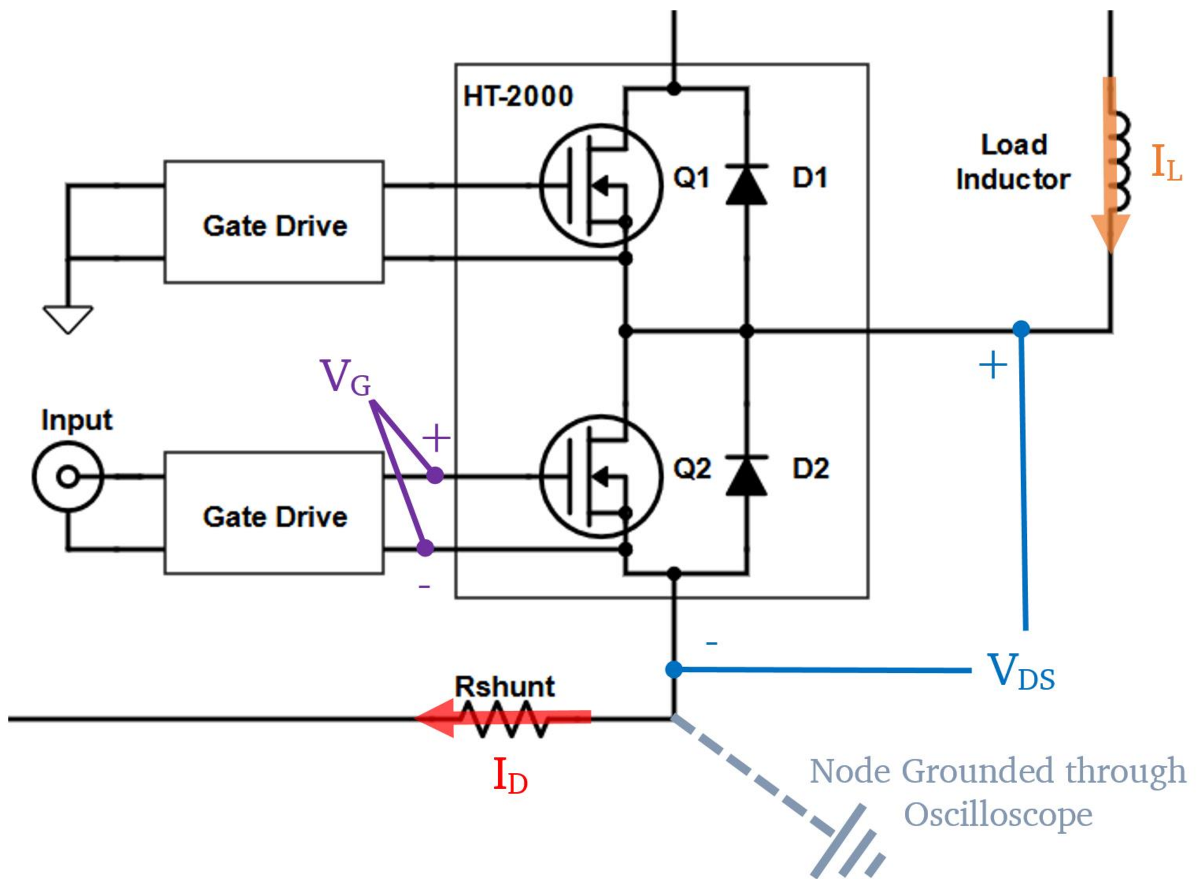

Figure 28: Measurements of Double Pulse Test

For the HT-2000, V_G was measured with a 10:1 ground-referenced probe connected to the gate drive module; V_{DS} was measured with a high voltage 100:1 ground-referenced probe; I_D was measured via the voltage drop of a 100 mΩ shunt resistor; and I_L was measured with a current transformer. The reference node for the V_{DS}, V_G, and I_D measurements (as indicated in Figure 28) is connected by the shields of the coaxial cables through the oscilloscope to earth ground. For this reason, the negative bus of the capacitor bank is not tied directly to ground but floats near zero volts. To prevent ground loop currents during DPT, the high-voltage power supply should not be ground referenced either.

DPT gives a time domain standard against which SPICE models can be compared and calibrated. Test parameters such as bus voltage, drain current (I_D), junction temperature (T_J), and gate resistance (R_G) can be matched to the final system to ensure model accuracy under those conditions. One important function of DPT in this modeling methodology is tuning of the common source inductance (L_{CSI}), a parameter which is difficult to measure with an impedance analyzer. Finite element analysis of a detailed model could produce this value with better confidence but is not universally accessible, and the model's accuracy indicates that FEA is not mandatory.

4.1. Development of Test Stand

Conducting DPT requires designing and fabricating a test stand [1],[54]. The modular test stand used to analyze the HT-2000 is depicted and annotated in Figure 29. This DPT stand can operate at bus voltages above 1 kV, at load currents of several hundred amps, and can accommodate most power modules or discrete-packaged semiconductors by replacing the interface board shown on the right-hand side of figure 28. The capacitor bank supplies energy during the test. The white contactors control the connection of the capacitor bank to the power supply for charging, and can also connect the bank through dissipative resistors to the negative bus terminal, allowing quick discharge after testing. Additionally, high-value resistors across the bank slowly but continuously discharge it, a safety precaution ensuring that the bank will not remain energized. The CIL test stand also includes a protection circuit which isolates the device-under-test (DUT) if excessive bus current is detected. More details on the design of this test stand can be found in [55].

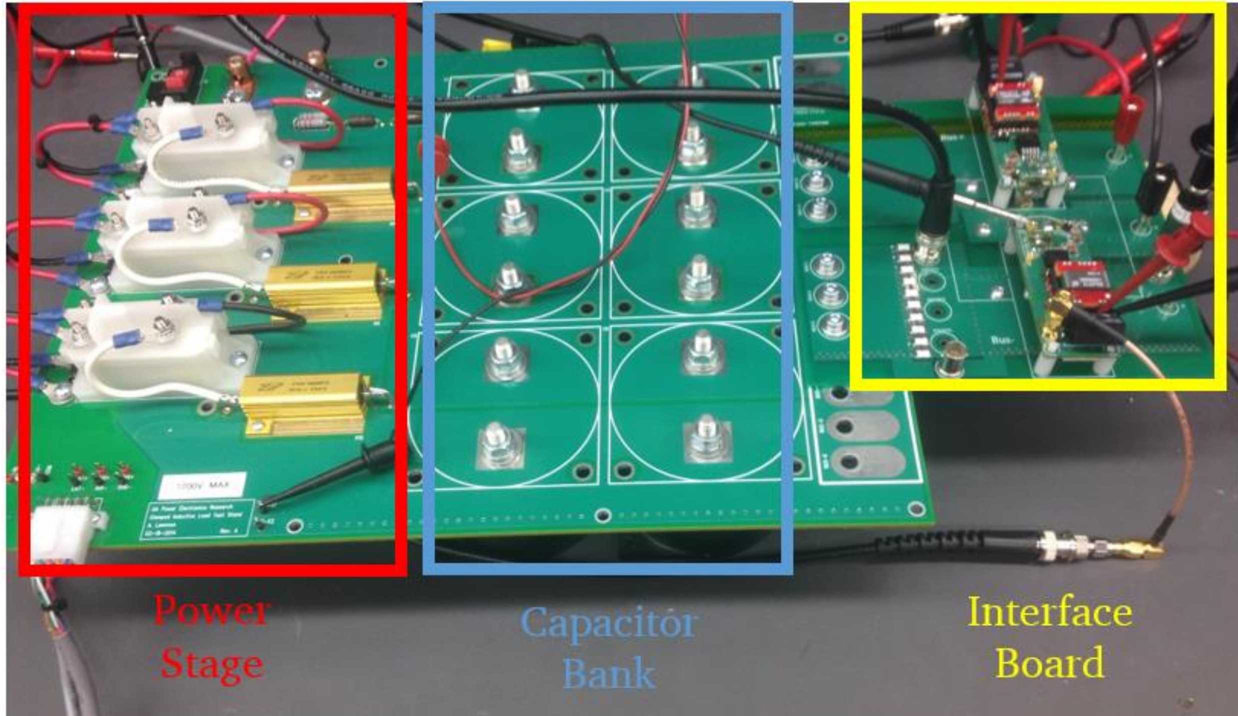

Figure 29: CIL Test Stand

4.1.1. Metrology Considerations

Bus inductance plays an important role in power electronics system dynamics, especially for WBG systems. During switching events, changes in current (di/dt) and voltage (dv/dt) cause ringing because the system's parasitic inductance can rapidly exchange energy with the semiconductor intrinsic capacitances [25]. The high switching speed of WBG power modules, coupled with their high current capacity, dictate that even small inductances can contribute to undesirable dynamics. This underdamped ringing not only degrades performance in converters, but also complicates DPT measurements. This also obscures the desirable dynamic performance of these modules with undesirable parasitic-driven system behavior [12],[17]. An additional side-effect of this phenomenon is that the maximum peak voltages observed during ringing events require lower

oscilloscope resolution to prevent clipping. In addition, voltage overshoots that exceed the rating of the semiconductors can destroy the DUT. For these reasons, the test stand requires wide bus-work, reliable connections to the DUT, and dense vias when implemented on multiple layers.

Measuring bus current also requires careful consideration or the implementation can counteract the benefits of low inductance bus-work. For example, routing the current through a BNC style shunt or the center of a current transformer introduces a constriction which increases the inductance of the bus. To counter this, a low inductance shunt resistor was designed into the test stand. Figure 30 shows that the shunt is composed of twenty SMD resistors evenly spread across the negative bus (additional resistors are soldered to the bottom of the PCB). Together, the twenty resistors which make up this shunt, total 100.34 mΩ, leading to a .10034 volts-per-amp conversion factor. Most oscilloscopes, including the Tektronix MDO4054 used to measure the HT-2000, only allow integer probe ratios. This introduces a .3% error into the current measurement, but this error could be removed during analysis through software.

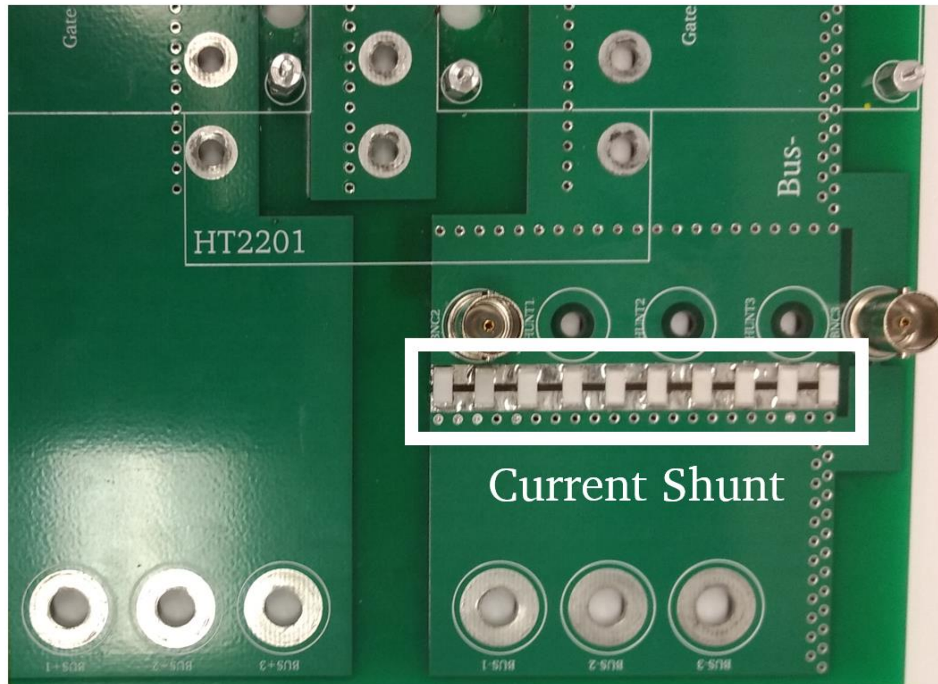

Figure 30: Current Shunt

In addition to careful design of the test stand PCB, instrumentation must be carefully selected to accurately capture system dynamics. For the analysis of the HT-2000, voltages were measured using ground referenced probes with a minimum 200 MHz bandwidth. In addition, ground connections were not made with alligator clips, which introduce additional inductance to the measurement path; instead, soldered wires and PCB-mount probe sockets were used to keep the measurement loop minimized.

4.1.2. Gate Drive Signal Generator

To perform CIL testing, a specialized signal is required for the active switch gate drive to generate the double pulse test sequence. Figure 31 shows an example DPT gate signal (V_G), and the corresponding inductor current (I_L). First, the switch is turned on to charge the load inductor, a process typically requiring 20 to 100 µS (depending on the desired current set point, inductor size, and bus voltage). The switch then turns off for a

specified off-time, and then on for a secondary pulse of the same duration, and finally back off. Only the first turn off and the second turn on are of interest; these events have approximately the same current bias and correspond to a single switching cycle of a converter under load at steady-state. Because of the brevity of the DPT sequence, device failure is less likely than in a full converter.

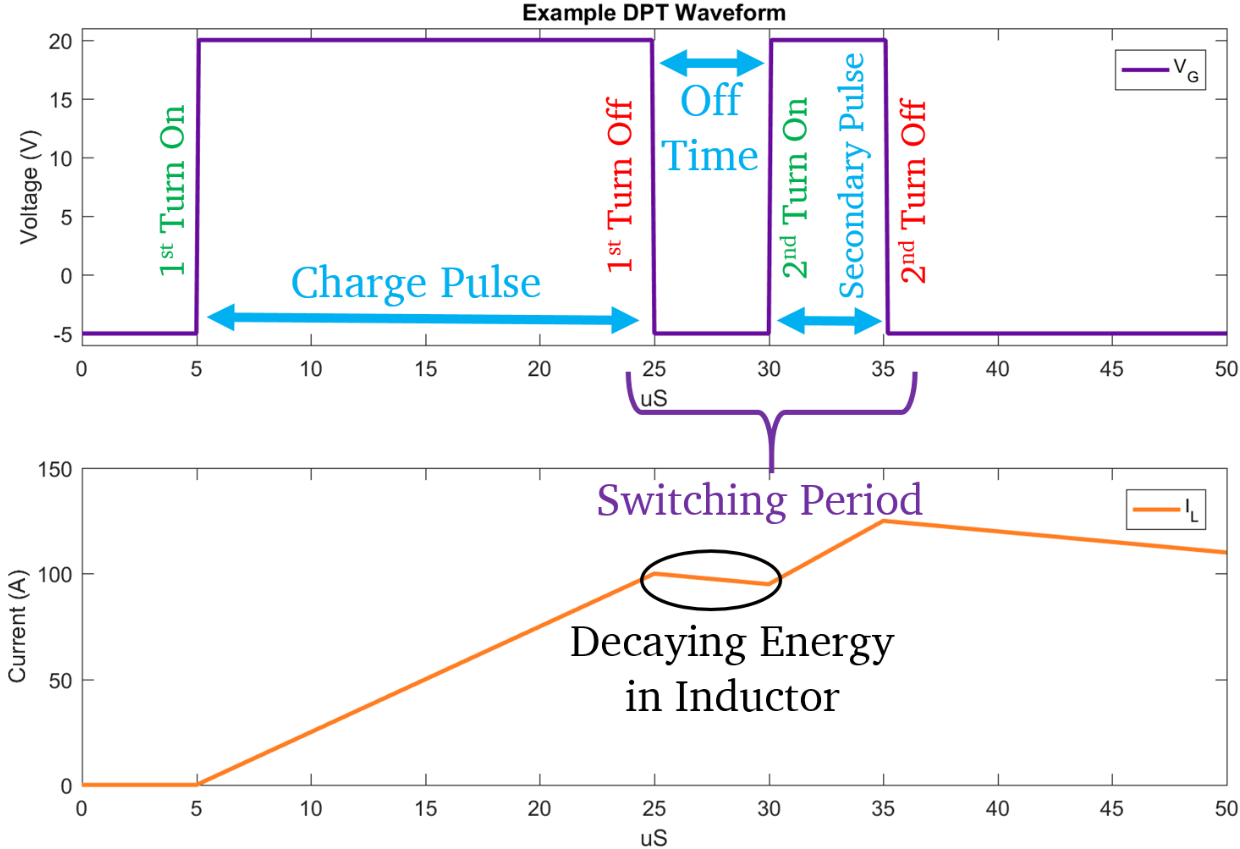

Figure 31: Example DPT Waveform

The length between pulses and duration of the secondary pulse correspond to the switching frequency of the simulated converter; the duration of the switching period shown in Figure 31 (10 μS) is equivalent to 100 kHz. The on and off pulse time, or switching frequency, must be selected carefully for DPT to deliver usable results. Pulse time must be long enough for the system ringing to subside, but short enough that the

current at turn off and turn on is similar. While the semiconductor is gated off, magnetic energy stored in the load inductor will be dissipated by the inductor winding resistance and freewheeling diode; the falling I_L in Figure 31 reflects this lost energy. For the HT-2000, a 10 μS switching period gave sufficient delay for system ringing to subside without excessive loss of magnetic energy stored in the load inductor.

Previously [55], the DPT gate signal was generated by an arbitrary waveform generator, specifically the Tektronix AFG3252C. However, this instrument is not ideal for CIL testing because scaling the charge pulse length changes the timing of the secondary pulses. If changing current set point also modifies switching frequency, comparisons become more challenging. A time-consuming solution is programming an arbitrary signal for each current, but a better option is a system which can accept any charge pulse duration while leaving the secondary pulses unscaled. Figure 32 shows the system developed. The Microchip Explorer 16 dev board generates a DPT signal in response to a user input specifying the charge pulse duration. A high-speed gate drive IC is used to drive the 0-5 V input of the gate drive with the 0-3.3 V output of the microcontroller.

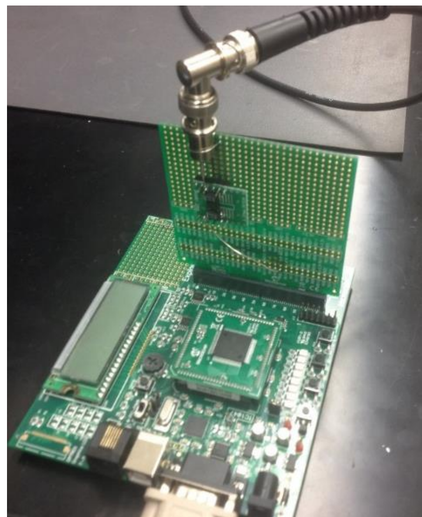

Figure 32: Custom Pulse Generator

4.1.3. Load Inductor Design

In double pulse testing, it is ideal for the load inductor to have a SRF above the frequency of the system ringing. If this is not the case, the SRF of the load bank may be excited by the MCPM switching transitions and contribute to the system ringing. Additionally, larger inductance allows finer resolution in current set point. This is because a large inductor's current bias changes slowly, requiring a longer charge pulse to achieve a given current set point. This longer charge time means that the minimum resolution of the signal generator will make smaller changes to current, and more accurate set points can therefore be achieved. Another advantage of a larger inductor is more stored magnetic energy, such that the load current decays more slowly during the off interval. Finally, an ideal inductor will not saturate at the DUT's maximum current. Considering these design criteria, a suitable load inductor for the HT-2000 test stand requires at least 100 μH inductance, a 350 A current capacity, and a SRF of at least 30 MHz. A commercially-available inductor with these specifications was not found, so a custom load inductor bank was designed and fabricated.

In general, a set of distributed inductors has a higher SRF than an equivalent-valued single inductor. Equation (24) shows that the self-resonant frequency is inversely proportional to the square root of inductance and equivalent parallel capacitance (EPC), so a smaller inductor will have a higher SRF if EPC is unchanged. The impedance of two inductors in series is additive. This means that while the equivalent inductance of the two will increase linearly, the change in SRF is more complex. In practice, the resonant peaks from both individual inductors will manifest in the total, series-combined impedance.

Figure 33 plots two inductors with different resonances (1.55 MHz and 11.2 MHz) against their series combination, illustrating how the impedance at each frequency is combined. Thus, the series combination of two inductors with the equal SRF will have the same SRF. Considering the problem mathematically, small inductors in series are superior to a single large inductor.

$$SRF[Hz] = \frac{1}{2\pi * \sqrt{LC}} \tag{24}$$

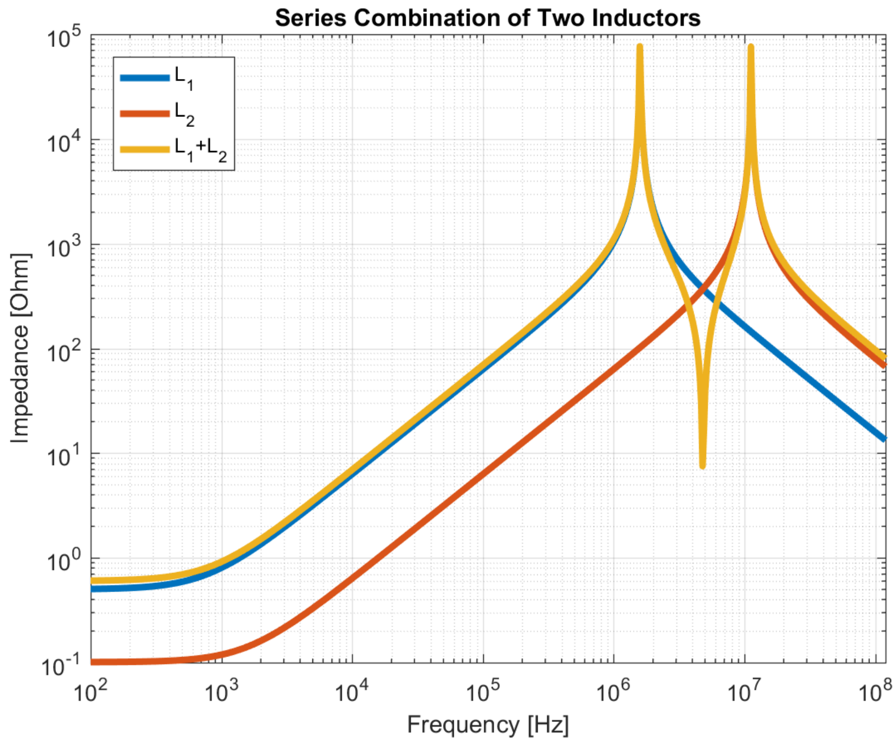

Figure 33: Demonstration of Series Inductors' Additive Impedance

One important step in the design of the load inductor was optimizing the small component inductors which would subsequently be combined into the load bank. An important design choice for any inductor design is the selection of a core material. While air core inductors do not saturate, the lower permeability of air requires more turns and longer wire lengths to achieve the same inductance as an inductor wound on a high-

permeability core. Longer wire also creates higher ESR, and results in higher conduction losses. Because pulse timing in DPT is typically dictated by ringing, higher ESR leads to greater difference in current at the turn off and turn on events. Keeping ESR low was deemed more important than the risk of saturation, so high frequency ferrite-based cores [61],[62] were chosen to implement the load bank inductors. Because 11 cores were available at the time of assembly, the target inductance of each element was 10 to 15 μH.

Another important design step was minimizing the EPC of the small inductors to achieve maximum SRF. Many inductor designs were wound and empirically evaluated to study causes of parasitic capacitance, and three sources of EPC were found to be significant. First, the inductor leads must be spread apart to reduce inter-lead capacitance, as shown by the winding in Figure 34, which fills two thirds of the core. Second, the coupling between adjacent turns contributes to inductor EPC. However, since the number of turns is dictated by the required inductance, this contributor to EPC can only be reduced by spacing the turns evenly. These parasitics must be balanced; using less of the core leads to higher inter-winding capacitance, and using more of the core leads to higher inter-lead capacitance. Third, it was discovered that spacing the conductor away from the core increased the SRF of the resulting inductor, indicating capacitive coupling can occur through the core itself.

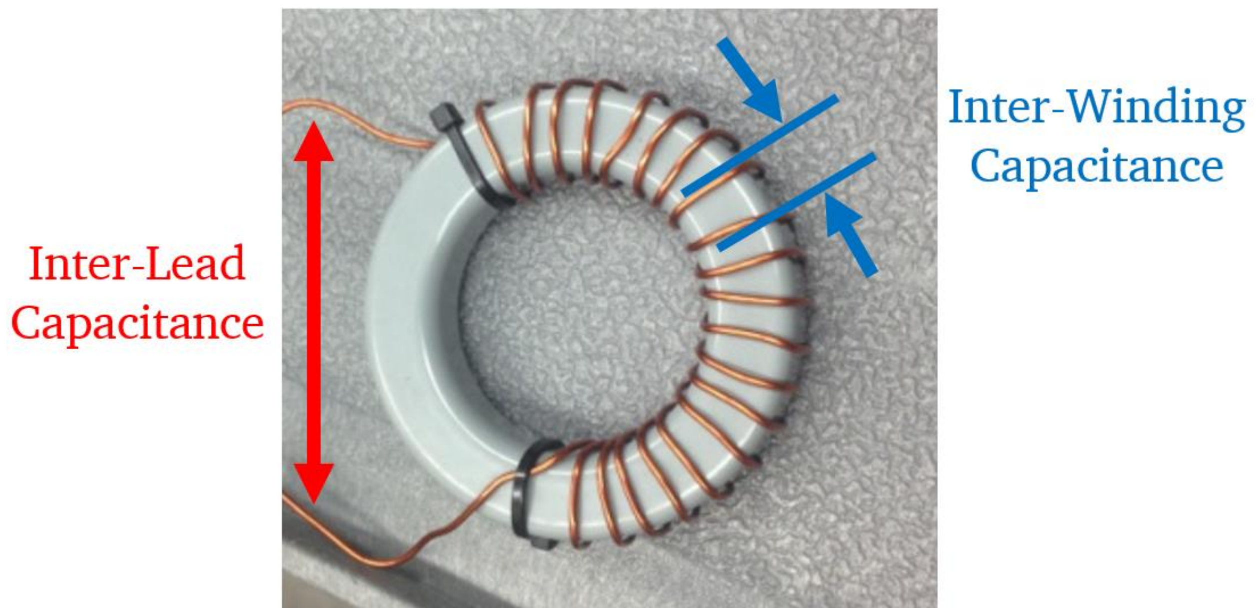

Figure 34: Initial Toroidal Inductor

Based on the outcome of this parametric study, the improved inductor element of Figure 35 was created. This inductor's core is sheathed in plastic wire loom to reduce capacitive coupling between the winding and core. Additionally, the wire loom provides ridges to evenly space turns about the core. Wire gauge had little effect on SRF, so the final inductor design uses 14 AWG wire (instead 16 AWG) to improve current handling. These improvements increased the SRF from 18 MHz to 49 MHz (shown in the appendix, Figure 54 and Figure 55).

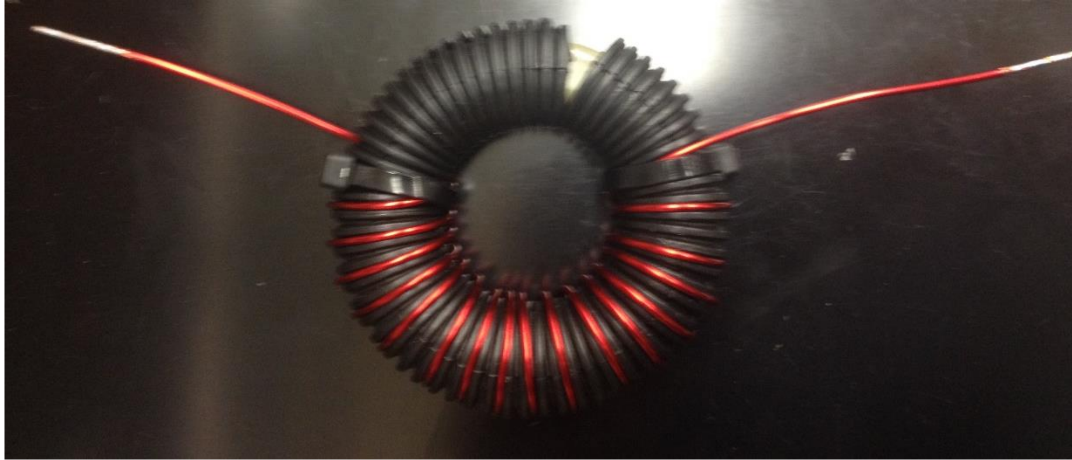

Figure 35: Improved Toroidal Inductor

Figure 36 shows the two load banks constructed from these toroidal inductors. The ABS plastic frame holds each inductor, allowing for easy transportation and spacing them apart to prevent magnetic or electrical coupling. A bottom piece of ABS is mounted to the top frame by standoffs, providing rigidity and spacing the inductors off the test bench. Between each inductor is a banana jack to allow easy reconfiguration of the series-connected inductors.

Figure 36: First Bank Under Construction (Top), Completed Banks (Bottom)

The E4990a ZA struggles to measure long conduction paths at high frequency. To characterize the entire load bank shown in Figure 36, a multi-step approach was adopted. First, each inductor was individually measured and an equivalent circuit model was created for each. Second, these individual models were combined in LTspice. The impedance of this series combination of inductor models is shown in Figure 37. The completed load inductor bank incorporates 16.5 m of wire and measures 140 μH, 145 mΩ of ESR, and a SRF of 31 MHz. Time domain testing showed minimal saturation at 350 A load current. Overall, the load bank satisfies the design criteria established for testing the HT-2000.

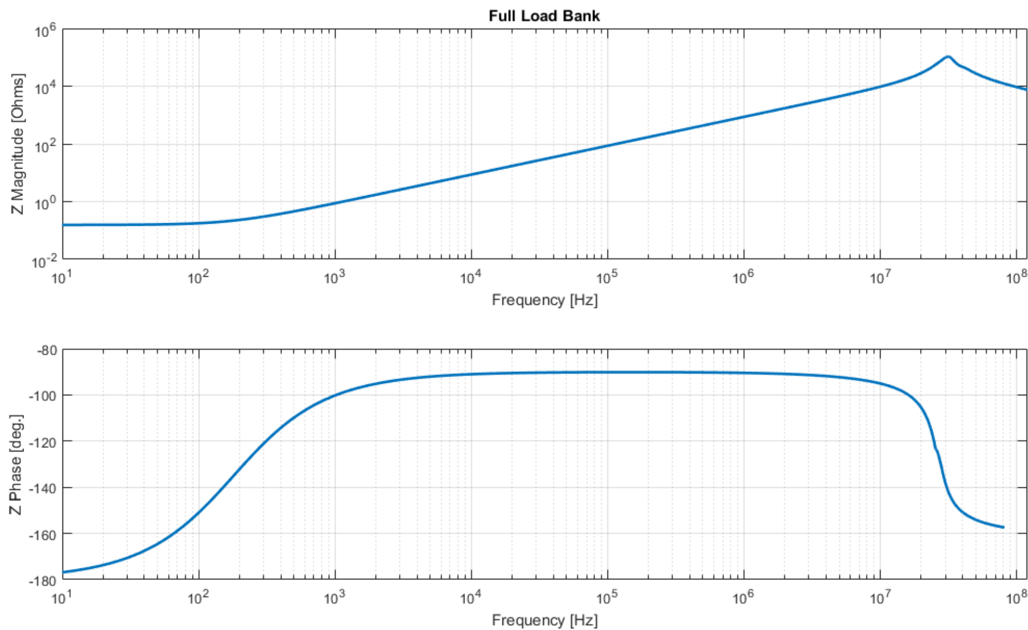

Figure 37: Load Bank Impedance (Series Configuration)

4.2. Parameters of Dynamic Testing

Many parameters dictate the behavior of semiconductors during double pulse testing, including junction temperature, gate resistance, drain current, and bus voltage. Full characterization of a MCPM requires careful study across all operating points for each

parameter. However, system designers can keep testing manageable by designing around specific operating conditions.

While temperature is an important factor in semiconductor behavior [7], room temperature testing of the HT-2000 was deemed sufficient to validate the proposed methodology. To measure under the elevated thermal conditions expected for a converter, a hot plate can be mounted to the baseplate of the module and the junction temperature raised to the desired thermal set point. Comprehensive analysis would parametrically sweep thermal conditions for all electrical operating points; the data could then validate the model's predictions of response to thermal changes. However, evaluation of the MCPM under study at elevated temperatures was considered tangential to the primary goals of this thesis; the parasitic elements which constitute the primary focus of this work are not expected to have significant thermal dependence.

Gate resistance significantly influences the rate of change during switching events; higher gate resistance causes slower switching events, which is safer for the module but also increases switching losses [56]. To reduce risk to the HT-2000 under analysis, DPT was first conducted with a conservative 10 Ω resistor, and later with 5 Ω and 2 Ω gate resistors. In general, if the final system's gate resistance is known, the model could be fit to those conditions exclusively. While it requires more work to fit the model to multiple gate resistors, doing so increases confidence in the model's accuracy and demonstrates that it can predict more than a single point of operation.

Conducting DPT at multiple current set points within the device rating is also important for model validation. It is important for the model to accurately predict

behavior across load currents, which vary significantly by application. The drain current is managed by the size of the load inductor, the applied bus voltage, and length of the charge pulse. Because the load inductor dictates drain currents, the current is determined by volt seconds divided by inductance. The required charge pulse duration for each drain current was computed with Equation (25). Since operating at higher drain current values introduces additional risk to the DUT, for each gate resistor the HT-2000 was first tested at 100 A, then 275 A, and finally 350 A (the maximum rated current for this module configuration).

$$v = L\frac{di}{dt} \Rightarrow i = \frac{\int v * dt}{L} \tag{25}$$

MCPM's are often tested at half their rated voltage to ensure sufficient margin is available for the high voltage ringing on V_{DS} during switching events. Since the HT-2000 is rated at 1.2 kV, all CIL tests were performed at a bus voltage of 600 V. To reduce the risk to the HT-2000, each test was started with a 50 V bus, to validate the gate drive and switch operation. The bus was then incremented by 50 V and the test was repeated. While checking for shoot through current, which occurs if both switches turn on simultaneously, the process was iterated until 600 V was reached.

In total, the HT-2000 was tested at 600 V with 10 Ω, 5 Ω, and 2 Ω gate resistors. For each value of gate resistance evaluated, DPT results were collected at drain current values of 100 A, 275 A, and 350 A. Though riskier, the HT-2000 could also be tested at 800 V or with a 1 Ω gate resistor, but the tests conducted cover most electrical operating conditions and give an overview of the module's dynamic behavior. Figure 38 and Figure

39 show the operational test stand. During testing, a clear polycarbonate blast shield is placed around the system to protect operators from dangerous mishaps and to reduce the accessibility of high voltage terminals. The capacitor bank is controlled using a wired, but electrically isolated, remote-control box to operate the charge and discharge contactors. The DPT sequence is initiated by sending a serial command from a computer to the microcontroller board. The microcontroller responds by generating the requested gate-drive input signal, and then the gate drive circuit switches the module.

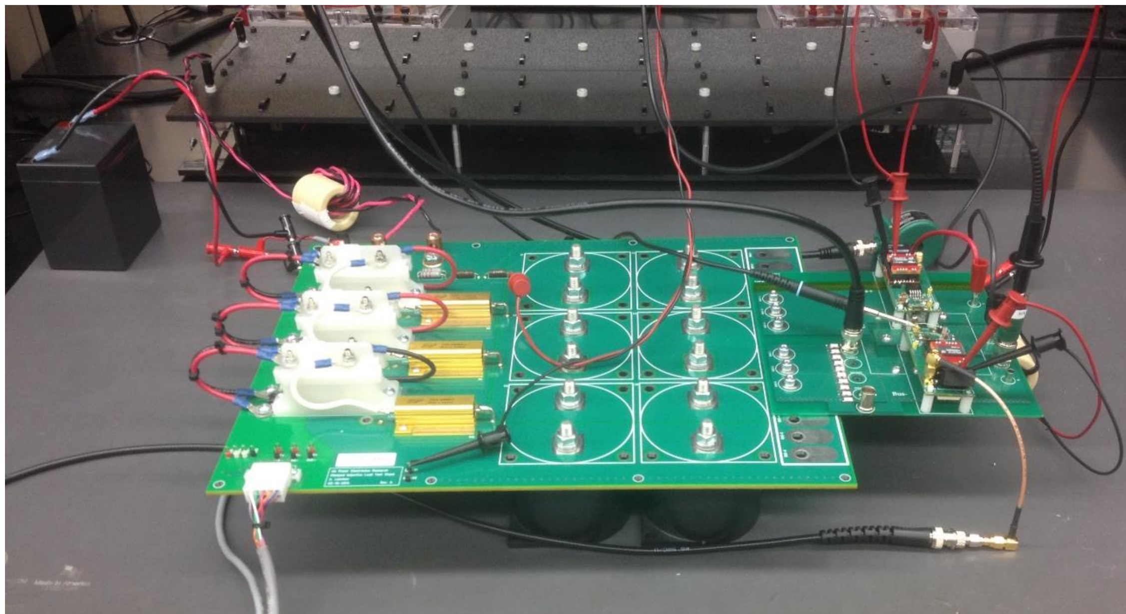

Figure 38: Complete CIL Test Stand

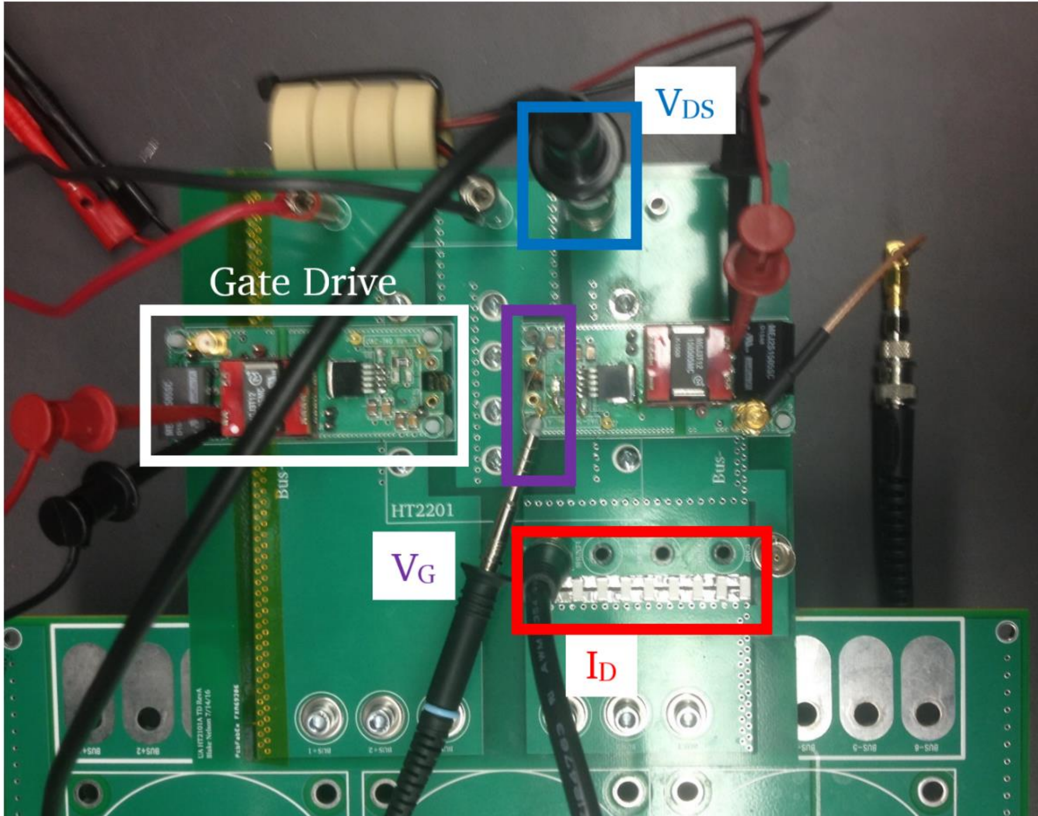

Figure 39: Overview of HT2000 Adapter Board

4.3. Switching Results

A set of typical DPT waveforms observed during this work are shown in Figure 40. This test of the HT-2000 was conducted at 600 V bus voltage, 100 A load current, and used a 10 Ω resistor. Both V_{DS} and I_D contains parasitic-induced ringing at turn-on and turn-off. However, with only 220 V overshoot in V_{DS} at turn-off and 50 A overshoot in I_D at turn-on, this ringing is considered modest for a high-performance WBG system. As described previously, these peaks must be carefully monitored to ensure they do not surpass module ratings. Brief spikes (50 to 100 nS) above the ratings of a module are unlikely to cause damage, but sustained ringing or excessive overshoots can destroy the DUT. Additional results can be found in the Appendix (Figure 56 and Figure 57).

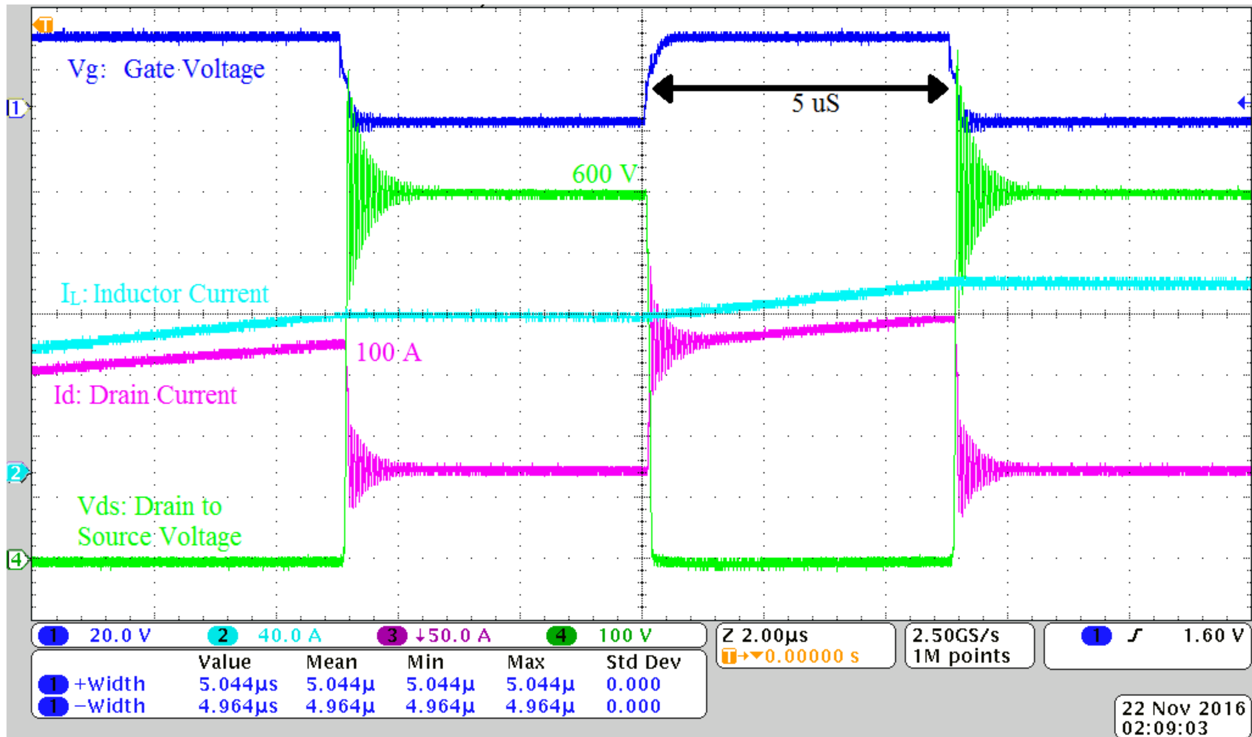

Figure 40: CIL Waveform: 600 V DC bus, 10 Ω Gate Resistor, 100 A Load Current

The instantaneous power dissipated by the module during switching is calculated by multiplying V_{DS} and I_D at each time-step. Switching losses are then computed by integrating this instantaneous power waveform over the turn-off or turn-on interval. The calculated switching losses for turn-off is 2996 µJ and for turn-on is 2700 µJ. The downward sloping switching energy shown in Figure 42 suggests the accumulation of negative power. This is a measurement artifact which results from error in the V_{DS} waveform. Because of the scale of this measurement, 250 V/division, the oscilloscope indicates a small negative bias (a few volts) when V_{DS} was slightly above zero due to the voltage drop across the conducting MOSFET. This error, multiplied by the high drain current results in a small negative power and the decaying energy within the integration window. In this case, the peak switching energy is more accurate than the final value.

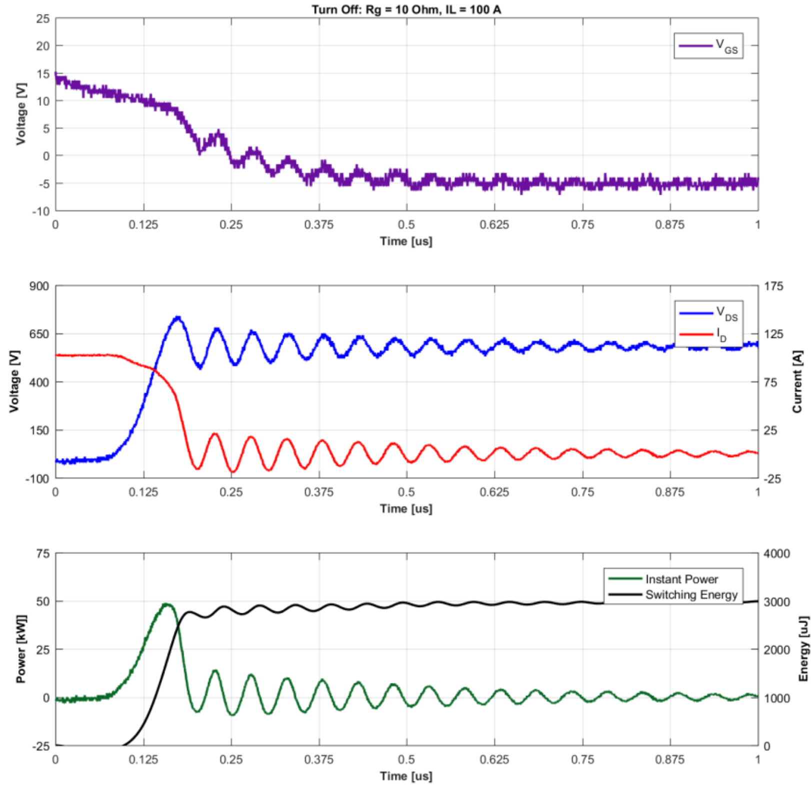

Figure 41: Turn-off Switching Energy, R_G 10 Ω, I_L 100 A

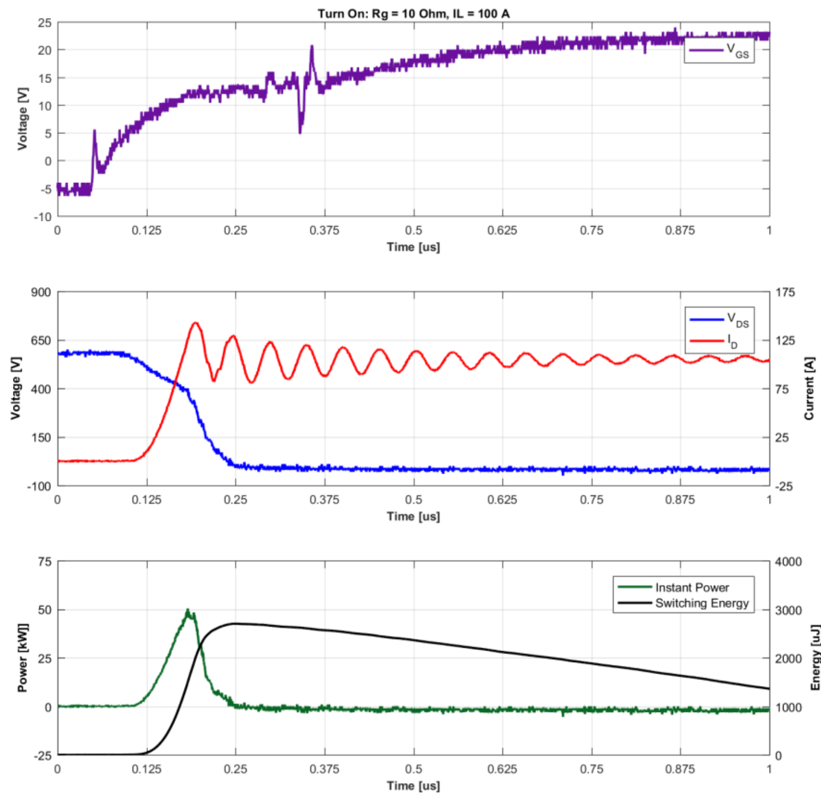

Figure 42: Turn-on Switching Energy, R_G 10 Ω, I_L 100 A

CHAPTER 5:

SPICE MODELING

In order validate the parasitic model developed in Chapter 3 with the transient results of Chapter 4, one additional step is needed. The parasitic model must be combined with a suitable model of the semiconductors within the MCPM to evaluate the transient behavior of the model through time-domain simulation. The HT-2000 was modeled using LTspice, a graphical circuit simulation tool available from Linear Technologies, which is commonly used in design of power electronics applications. To create this SPICE model of the HT-2000, a model of the semiconductor die was developed and extended to predict the behavior of the full MCPM. In addition, the DPT test stand described in Chapter 4 was characterized and modeled to enable direct comparisons between the simulation output and the DPT results.

5.1. Modeling of Die

The first component necessary for the implementation of a MCPM SPICE model is a suitable model of the semiconductor die (in this case, a SiC MOSFET and a SiC Schottky diode). These models may be provided by the MCPM manufacturer, but if not, a general model can be adapted. Manufacturers occasionally offer die models which can be implemented directly, but they more commonly provide SPICE models for discrete-packaged semiconductors. If the semiconductor manufacturer sells a discrete part built with the same die as the MCPM, the discrete part model can be reduced to a die model by

removing package parasitics. When neither option is available, static curves can be used to develop a behavioral model of the die. There are many generalized models available for this purpose [7],[19]-[22],[24],[57]; some of these models are optimized for accuracy and others are optimized for low computational complexity. A behavioral die model of the HT-2000 was available from the manufacturer [63].

The semiconductor die model can be implemented within the MCPM model in two ways. One possibility is to model each die within the physical MCPM separately. In the case of the HT-2000, this would require six MOSFET die per position, plus the associated interconnections. The other option is to perform area-factor scaling of the MOSFET die model, making it behave as a single large semiconductor die. For the HT-2000, the die model was area factor scaled (by a factor of six) because the computational complexity of the twelve die implementation resulted in simulation times extending from 10-30 seconds to several minutes. Although modeling each die individually should theoretically improve accuracy, this involves some practical challenges due to the size of the resulting system matrices. In addition, it is believed that the per-terminal impedance approach to parasitic modeling removes any potential advantage of the individual-die method. Theoretically, a more granular approach to modeling which captures the behavior of package structures and individual die positions could provide greater insight current asymmetry and other anomalies, but the difficulty of this approach is expected to be high.

After selecting and implementing a die model, it should be fit to the MCPM's static curves. Generic models require fitting, and manufacturer provided models can be improved with fitting. For the HT-2000, forward and transfer curves were used to tune the

manufacturer’s model (after scaling). The curve fit was optimized by a MATLAB routine which invokes LTspice through system commands, a process described in [64]. The genetic algorithm of MATLAB's Optimization Toolbox minimizes the difference between the model’s output from the measured static curves. This process was iterated until the fits of Figure 43 and Figure 44 were achieved. Finding an accurate parameter set is difficult because the model must predict many characteristics simultaneously, but because thousands of points can be swept automatically by MATLAB, the chance of finding an accurate parameter set is increased.

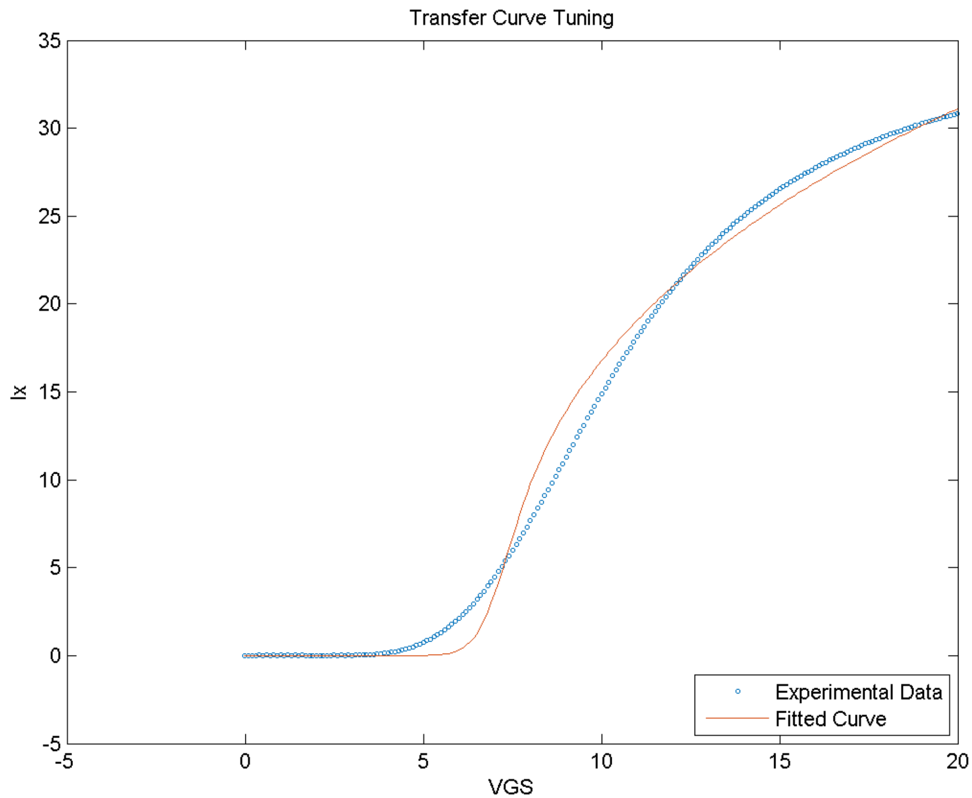

Figure 43: Fitted Transfer Curve

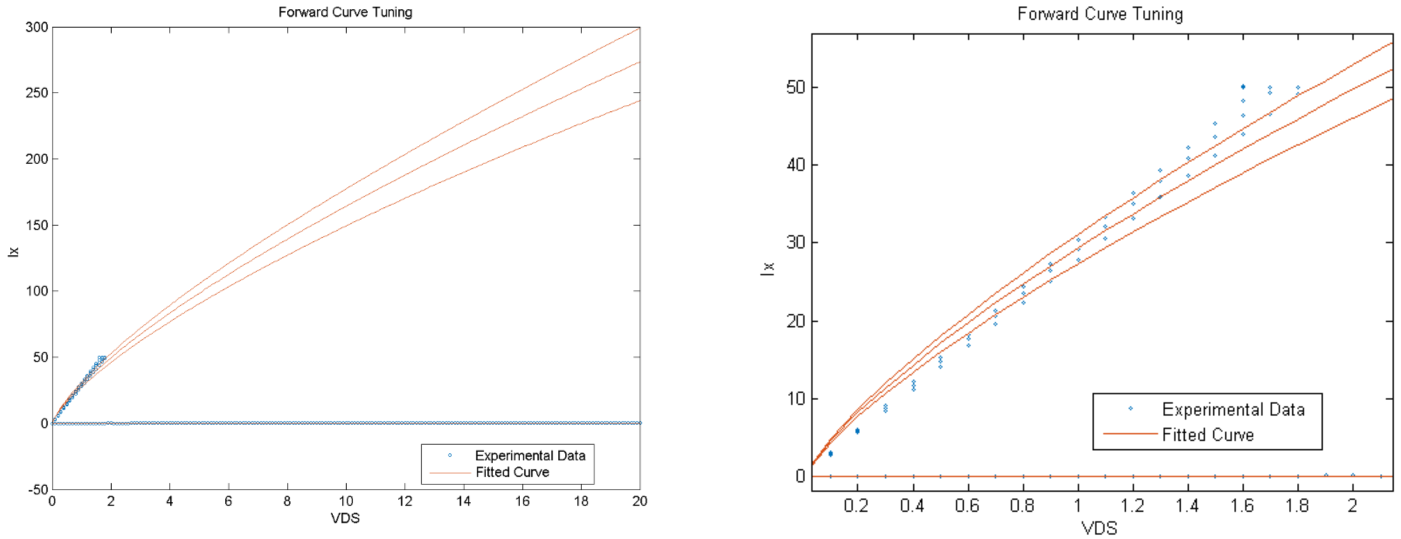

Figure 44: Fitted Forward Curve (a), Zoomed (b)

5.2. Modeling of HT-2000

To extend the SiC MOSFET die model into the MCPM model shown in Figure 45, packaging impedances, antiparallel diodes, and input terminals were added. C_1, C_2, and C_3 represent the parasitic capacitances between the module base-plate and the direct bonded copper (DBC) substrate regions, which can be estimated from ZA measurements. These capacitances substantially affect system dynamics if the base-plate is grounded. In DPT these capacitances have minimum impact because a heat sink is unnecessary. Most inductance values shown in the final model of Figure 45 are direct estimates from Chapter 3, but the final value for the common source inductance (L_{CSI}) was estimated by tuning the SPICE model to the DPT results. When L_{CSI2} is added, it must also be subtracted from L_{K2} and L_S to prevent discrepancy from the estimated values of Chapter 3. Similarly, L_{CSI1} must be subtracted from L_{K1} and L_P, but subtracting L_{CSI1} from L_P artificially reduces the inductance in the drain path of Q_2. Thus, an additional element (L_{D2}, which is equal to L_{CSI1}), is added to correct the value of inductance in the drain path of Q_2.

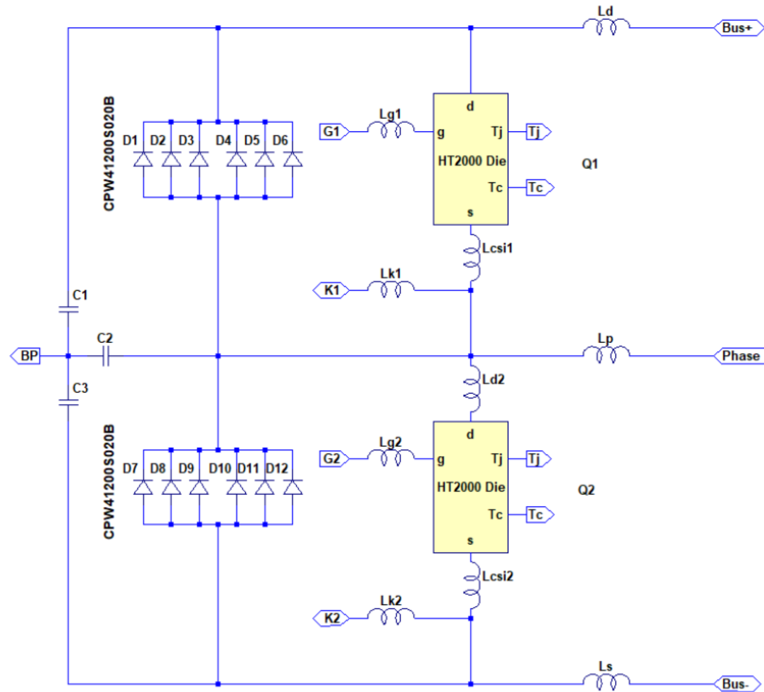

Figure 45: SPICE Model of HT-2000

The “HT2000 Die” SPICE block shown in Figure 45 is built on the manufacturer’s SiC MOSFET model which offers inputs for junction temperature (T_J) and case temperature (T_C) to account for the dependence of die behavior on temperature [7]. This model biases the junction and case temperatures of each die equally. The anti-parallel diodes are modeled separately, reflecting the separate diode die contained in the HT-2000. Some MCPM's rely exclusively on the body diode within the SiC MOSFET die and do not include separate anti-parallel diodes. These modules can be modeled with diodes embedded in the MOSFET die sub-circuit and do not require the inclusion of separate diode die models. The diodes in Figure 45 utilize a model provided by the manufacturer which is stored as a sub-circuit in the “HT2000 Die” block. The visual SPICE netlist shown in Figure 45 comprises a hierarchical block usable in other LTspice files; the terminals

shown in this figure allow connections between hierarchical levels. Figure 46 shows the graphical representation when this model is implemented in higher level netlists.

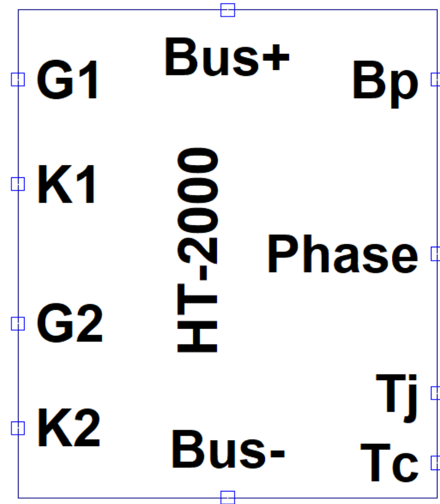

Figure 46: HT-2000. asy Drawing

5.3. Modeling of Test Stand

Figure 47 shows the model of the DPT test stand implemented in LTspice. The parasitics of the main test stand PCB are modeled by L_{BUS} and R_{BUS}, which were measured using the impedance analyzer and a milliohm meter (GW Instek GOM-804). The shunt resistor was also measured with the milliohm meter. R_2 is required for convergence of the simulation and models the connection of the bottom bus to ground through the oscilloscope. V_1 and V_2 control the temperature set point passed to T_J and T_C in the SiC MOSFET die model internal to the HT2000 hierarchical block. Because DPT does not produce enough heat to increase the die temperature from ambient and because all tests were conducted at room temperature, these terminals are biased at 25 degrees Celsius. The gate drive function block simulates both the active and inactive channel gate drives. Parameter R_G is used to set the active channel's gate resistance, and L_{G1} and L_{G2} model the interconnection between the gate drives and the HT2000 terminals.

Figure 47: DPT Test Stand SPICE Model

Figure 48 shows the component-level view of the capacitor bank, which includes the published values for ESR and ESL of the high-quality film capacitors which make up this bank [65]. Because the power supply is disconnected before the DPT sequence begins, all energy available during the test is stored in this capacitor bank. Therefore, outside of charging the capacitors, the power supply has little impact on DPT results. Rather than modeling the charging process, the power supply is omitted, and the available energy is simulated by setting the initial voltage of the bank to the bus voltage (in this case, 600 V).

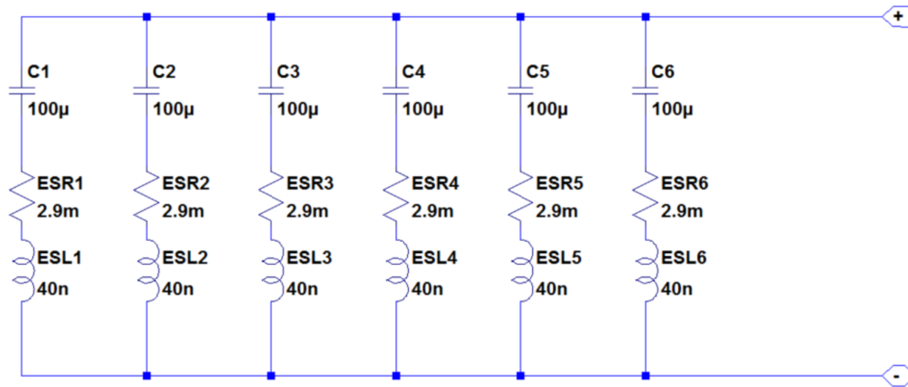

Figure 48: Cap Bank Model

Figure 49 reveals the conglomerated model which predicts the combined behavior of all 11 load inductors. The frequency response of this network is captured by EPR, EPC, and L. ESR represents the DC resistance, which dominates the impedance magnitude of the load inductor bank below 100 Hz. The value of ESR was confirmed with the milliohm meter, which is more accurate than the ZA for resistance measurements at DC. The behavioral voltage source, B_1, simulates the effect of gradual core saturation by decreasing the effective inductance of the combined network when current bias increases. B_1 only makes small changes below 350 amps and could be omitted from the model of the HT-2000, but it will be important in testing future MCPM's with higher current ratings.

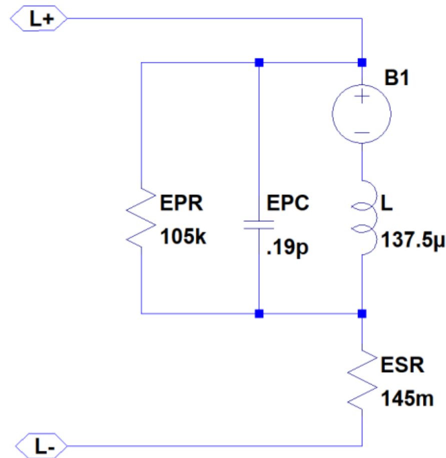

Figure 49: Load Inductor Bank

5.4. Tuning Model to Empirical Results

Because most parameters of the model are determined by characterization measurements, only a few variables require adjustment after the complete model is assembled. The estimation of common source inductance is the most important of these parameters, but gate resistance, gate interconnect inductance, and bus inductance also may require subtle adjustments to produce optimal agreement with experimental time-domain waveforms. Additionally, the timing of the gate drive signal must be carefully aligned to experimental waveforms. This process may require adjusting the charge pulse duration, off time, and secondary pulse duration. Gate timing mismatches should be addressed by adjusting the gate signal source; mismatches in V_{DS} or I_D should be addressed using other parameters.

Figure 50 shows the fit of the simulation output to the experimental data for the entire DPT switching cycle. The experimental data is drawn with solid lines while the simulated data is drawn with dashed lines. From this level, the simulation appears to fit the experimental data very well, but viewing the entire waveform obscures important

details. A closer look reveals the subtle discrepancies between the model prediction and the empirical waveforms.

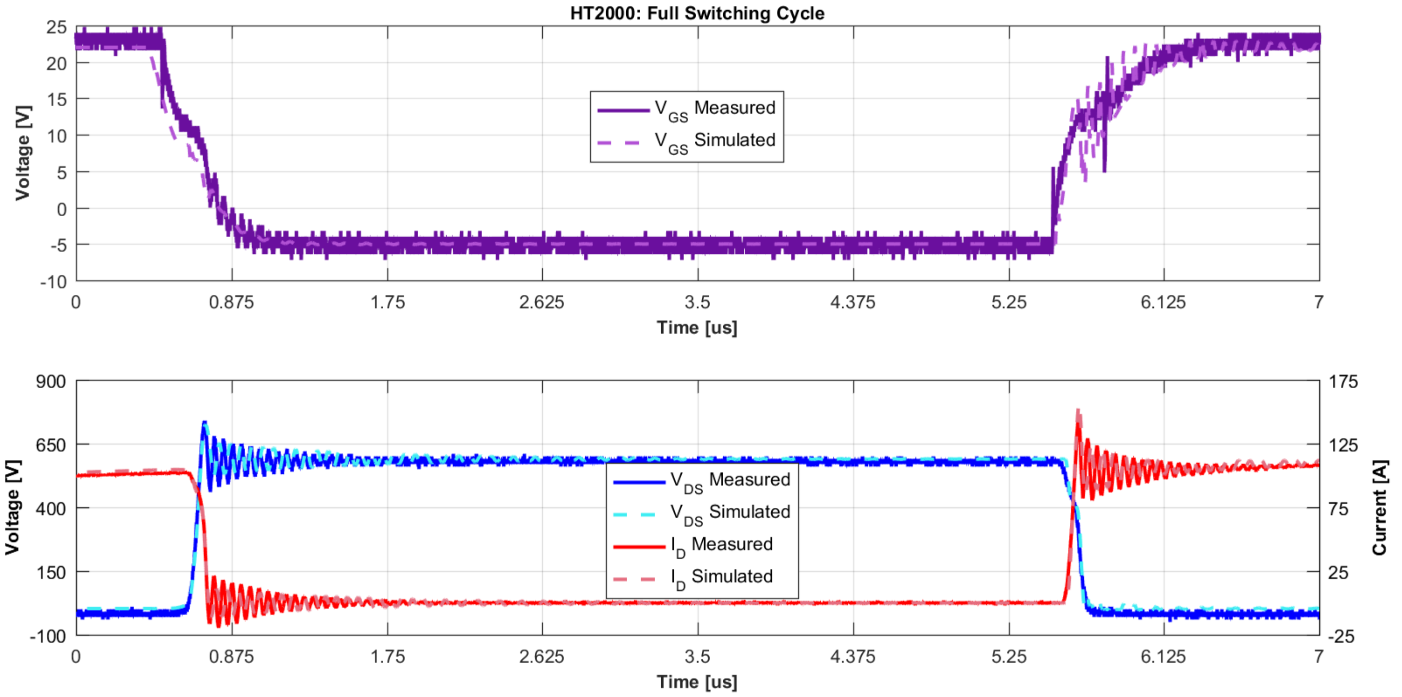

Figure 50: Full Switching Cycle

Figure 51 and Figure 52 focus on turn-off and turn-on events within the DPT, respectively. The edge rates observed during the current and voltage transitions represent the most important aspects of this simulation comparison. For these figures, not only are the rise and fall times of V_{DS} and I_D well-matched to the experimental data, but the overshoot in both V_{DS} and I_D is also within 10% of the experimental waveforms. Additionally, the damping ratio (or speed at which the ringing subsides) is very similar between the simulation and experimental waveforms.

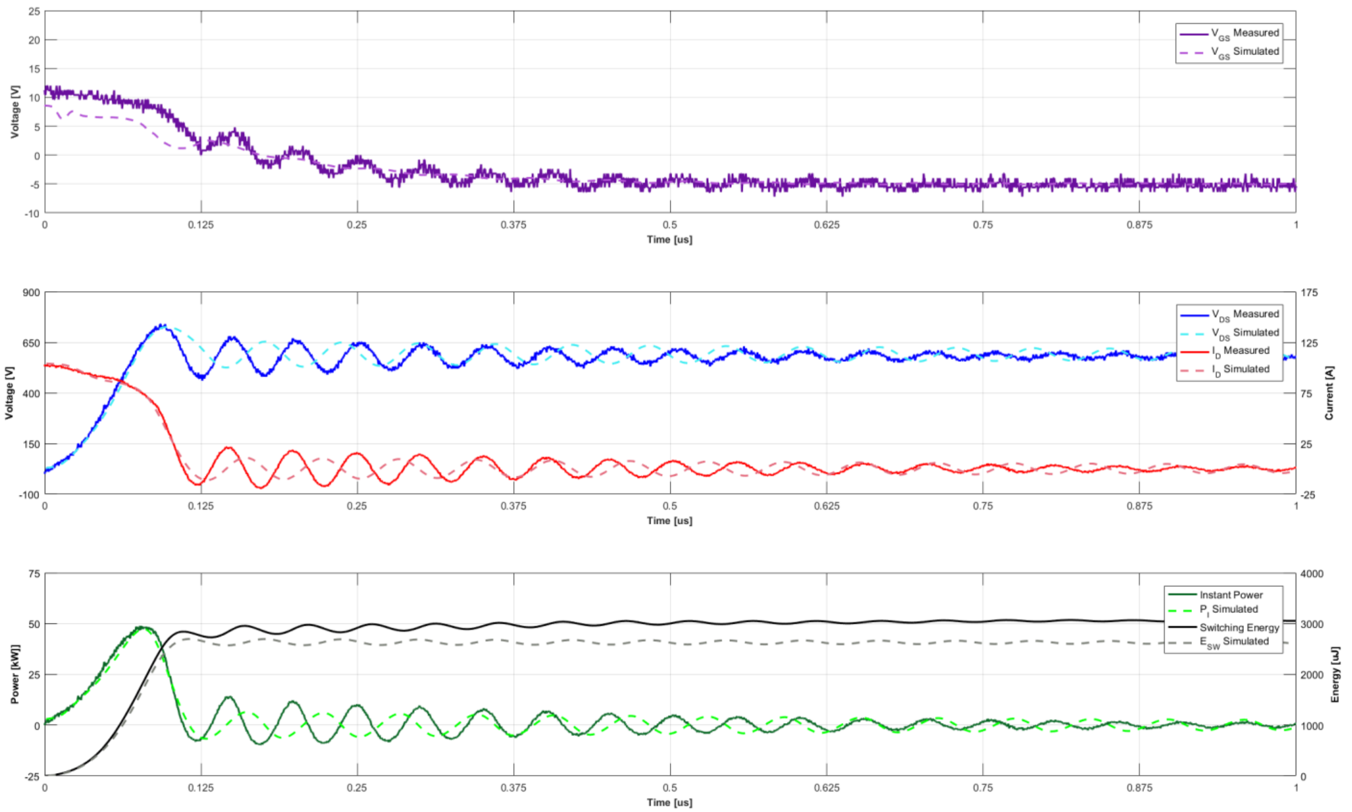

Figure 51: Turn-Off Event

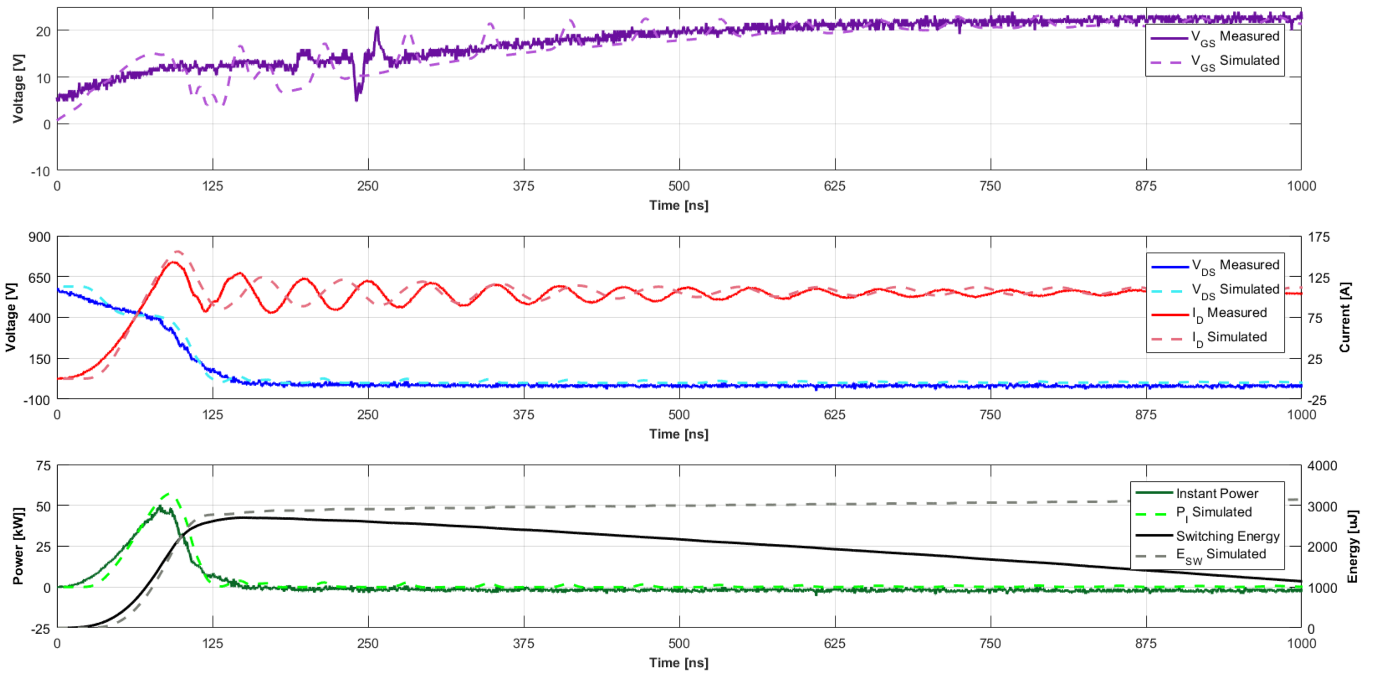

Figure 52: Turn-On Event

Table 5 lists the final parasitic elements of the HT-2000 model. Any values in this table which were adjusted during the final transient tuning are highlighted with red text. Interconnect parasitics include the packaging inductances estimated in Chapter 3 as well as L_{CSI}. The module base-plate capacitances were also measured for completeness, but have little impact on the simulation of DPT waveforms, because the baseplate is not grounded through a heat sink. The bus interconnect inductance, however, was reduced from the measured value. This reduction reflects the challenge of accurately measuring the large test stand PCB and potentially addresses inaccuracies in the fixturing used to perform this measurement. The gate inductance serves two purposes. First, it accounts for the interconnect inductance between the gate drive module and HT-2000 terminals. Second, it aids in modeling the non-idealities of the gate drive module itself. Because of this additional role, the simulation value (10 nH) is tuned above the measured value (3.6 nH).

TABLE 5
HT2000 MODULE SIC MOSFET PARASITIC PARAMETERS

Parameter	Measured	SPICE Value
INTERCONNECT PARASITICS (nH)		
L_D	2.3	2.3
L_{G1}	8.2	8.2
L_{CSI1}	-	2
L_{K1}	11.8	9.8
L_P	3.9	1.9
L_{D2}	-	2
L_{G2}	6.4	6.4
L_{CSI2}	-	2
L_{K2}	11.7	9.7
L_S	4.5	2.5
BASE-PLATE CAPACITANCES (pF)		
C_1	992	1000
C_2	989	1000
C_3	997	1000
BUS PARASITICS		
L_{BUS}	85 nH	50 nH
R_{BUS}	1 mΩ	1 mΩ
L_G	3.6 nH	10 nH

Legend:

Altered Value

Estimated from Time Domain

Four of the values in Table 5 (L_{K1}, L_P, L_{K2}, and L_S) were altered only by the reduction of L_{CSI}, leaving the total loop inductances unaltered from the values estimated from frequency-domain measurements in Chapter 3. L_{CSI} introduces negative feedback between the power and gate loops, reducing it allows for higher switching speeds, improved system dynamics, and reduced switching losses [8],[25]. L_{CSI2} plays a critical role in the shape and slope of V_{DS} and I_D during transition events and was the primary parameter for matching the simulated waveform to the time domain results. Because only Q_2 is active in the DPT, L_{CSI1} has no impact on the simulation, and both common source inductances were

assumed to be equal. In addition, L_{D2} exclusively accounts for the inductance removed from L_P and is therefore equal to L_{CSI1}. The critical importance of L_{CSI} means that even small changes will affect the simulation; for the HT-2000, changes of .25 nH were noticeable.

Figure 53 shows a comparison of simulated switching losses to empirical switching losses across load current. The model was tuned with the 100 A data and then compared to the two higher current data sets. Except for gate timing, which must be matched to the empirical gate signal, no model parameters were adjusted. In addition to the model's prediction of time domain behavior, the correlation of switching losses is empirical validation of the model.

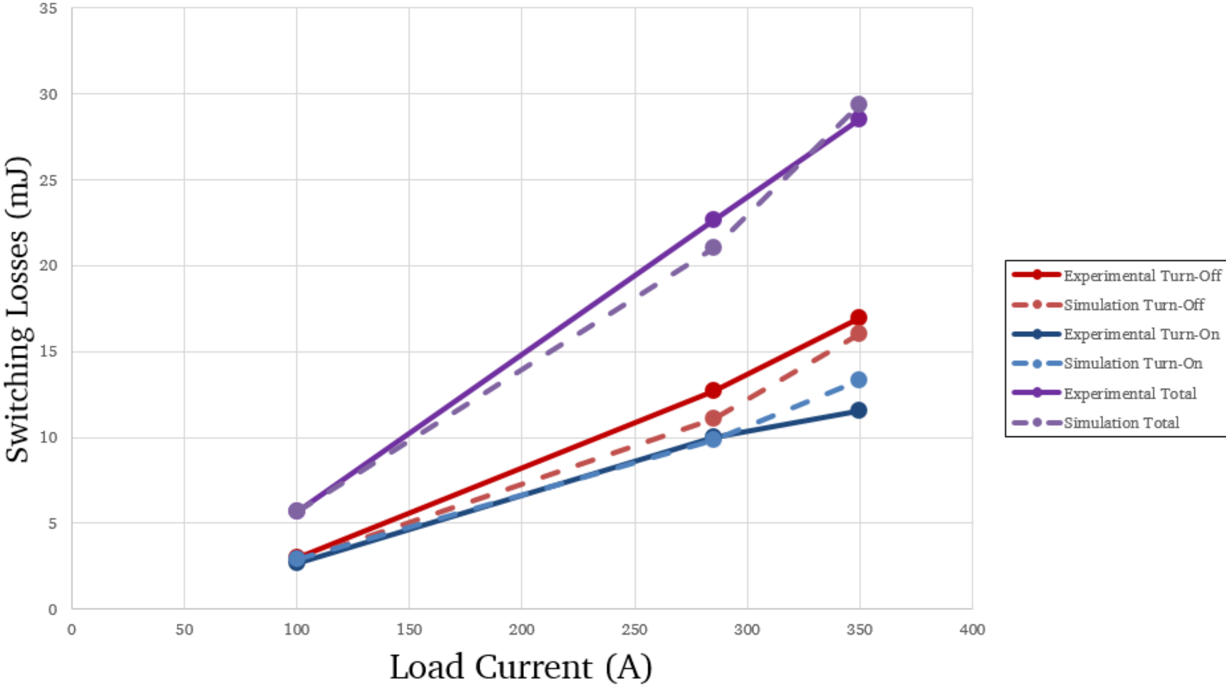

Figure 53: Switching Losses vs Load current; V_{DS} = 600 V, R_G = 10 Ω

CHAPTER 6:

CONCLUSION AND FUTURE WORK

6.1. Conclusion

The goal of this thesis is to synthesize a subset of prior work on modeling SiC semiconductors, modeling integrated modules, double pulse testing, and impedance analysis into a generalized methodology for modeling SiC MCPM's. The developed methodology creates a computationally lightweight model, but the empirical validation confirms the model is sufficiently accurate for power electronics design. The modeling process is organized by into three areas: parasitic extraction, time domain analysis, and SPICE implementation.

Parasitic extraction has previously been approached through many methods with varying degrees of difficulty and accuracy. Measuring packaging inductances with an impedance analyzer has been attempted previously, but the challenges introduced to the process by MCPM's merit more attention than most ZA applications. Accurate empirical measurements require carefully-designed custom fixtures and calibration, both of which are discussed in detail in this thesis. Additionally, little information is available in the literature to guide the quantification of error in impedance measurements using custom fixturing. As a result, new techniques and worst case simplifications were employed to create a first order approximation of uncertainty for the MCPM impedance models.

Double pulse testing is a common method for characterization of switching devices, but the high switching speed of SiC devices creates additional difficulties. For example, special consideration is required to minimize bus inductance in the test stand; otherwise, the behavior of the device under test can be obscured by the response of the test stand. Also, all instrumentation used must have sufficiently high bandwidth to capture the high-frequency content of SiC systems. Finally, the high voltage and current capabilities of SiC power modules mandate additional safety precautions not necessary for evaluating low-power systems.

Knowledge of power module design is needed to distil the assorted results generated by this procedure into a useful SPICE model for a MCPM. The developed per-terminal impedance model accurately describes the packaging impedance of the MCPM, even if it is significantly simplified from the organization of physical interconnects within the module. Additionally, the scaled die model can accurately predict the behavior of many parallel die at a much lower computational cost than separate models for each die. Finally, the prediction of common source inductance is critical to accuracy, and understanding its influence on device behavior is mandatory.

This thesis could not comprehensively capture all the aspects and minutia of the MCPM modeling process which has been developed at UA over the past two years. However, it is hoped that this thesis is detailed enough to offer an accessible method for end users to accurately model SiC power modules. Ideally, this thesis will decrease the challenge and investment required for system designers or manufacturers to model SiC MCPM's and improve accuracy of their modeling techniques.

6.2. Proposed Future Work

This section attempts to address the known shortcomings of the methodology presented in this thesis and to make recommendations on future improvements. Most importantly, it is recommended that FEA (or PEEC) should be conducted in tandem with ZA measurements. Not only would this offer confirmation to the measured frequency domain results, but it would also offer a means for directly estimating mutual inductance and common source inductance. Though it is the intent of this work to show that FEA is not mandatory for accurate MCPM modeling, it would improve the quality of the results and remove any remaining doubt regarding their validity.

Additionally, it is well known that temperature has a large impact on the behavior of SiC MOSFET's [7]. The primary focus of this work was to demonstrate a methodology for modeling MCPM parasitcs, which have minimal dependence on temperature. Therefore, the room temperature results show that a highly accurate model of MCPM parasitics has been developed. Many system designers will find it necessary to invest sufficient time to tune the temperature dependence of the SiC MOSFET die model. Although temperature dependence is tangential to the goals of this thesis, system designers should not ignore the relevance of temperature in simulation accuracy. A potential improvement to this thesis would be validating the models generated across a range of thermal conditions.

As another potential improvement, a more granular approach to modeling the parasitics within the MCPM structure could provide more precise prediction of power module behavior. In addition, each die could be individually modeled to study the impact

of variations in the semiconductors. Some preliminary work has been accomplished [66], but further work is required to empirically validate this improved methodology. Fully-resolving parasitics associated with individual connecting structures would likely be impractical due to the computational complexity of the resulting model. However, one further level of granularity beyond the "aggregated switch position" model presented in this work would likely be a significant improvement. The greatest advantage of this approach would be prediction of internal module behavior, which module designers could evaluate to further optimize MCPM design.

Finally, this methodology could be significantly improved with an alternate method of transient analysis for empirical validation of the parasitic model. While DPT is a common method for the evaluation of semiconductors and is extremely useful for validation of the SiC MOSFET die model, it is not the ideal approach for validating the parasitic model of the MCPM. Certain model parameters (such as L_D, L_P, and L_S) are largely obscured by the system response because the DPT test stand has bus inductances that are an order of magnitude higher than these values. Accuracy of the estimations for these parameters can therefore not be conclusively confirmed by DPT. Thus, in addition to DPT, an ancillary method of empirical validation for the parasitic model is needed.

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APPENDIX

A.1. Toroidal Inductors

Figure 54 shows the initial inductor design and corresponding frequency response measured by the E4990a. The SRF of the inductor is pointed out by the marker at 18 MHz. Note that the inductor windings are spaced evenly and occupy only two thirds of the core (mitigating two of the sources of parasitic capacitance discussed in Section 4.1.3). Ideally, the SRF of the inductor would be above 30 MHz to prevent it from being excited by the high frequency parasitic ringing.

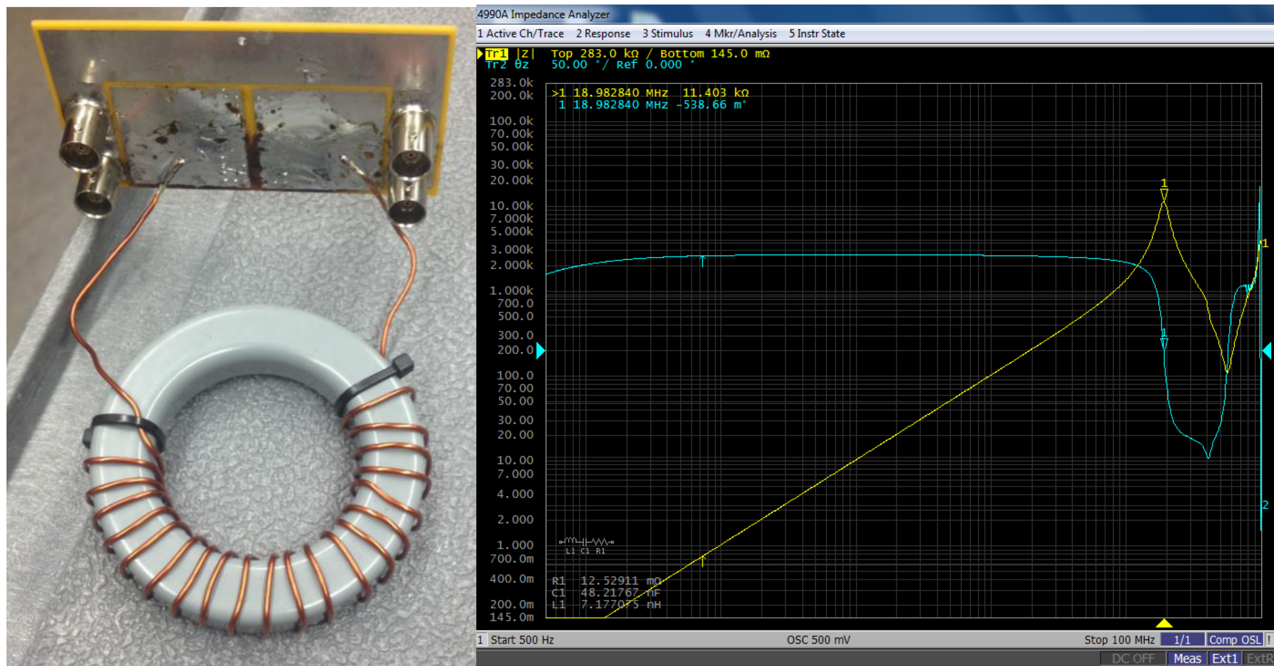


Figure 54: Initial Inductor (a), Frequency Response (b)

Figure 55 shows the improved inductor, which uses wire sheathing to space the windings away from the core. While study showed that this change is the main factor in

the increase of SRF to 49 MHz, a few smaller improvements were also made. The number of turns was reduced from 20 to 17, decreasing the inductance and inter-winding capacitance, both which decrease SRF. The inductance is still above 10 μH (the minimum acceptable per inductor for a sufficiently large load bank), so reducing the inductance was justified by the increase in SRF.

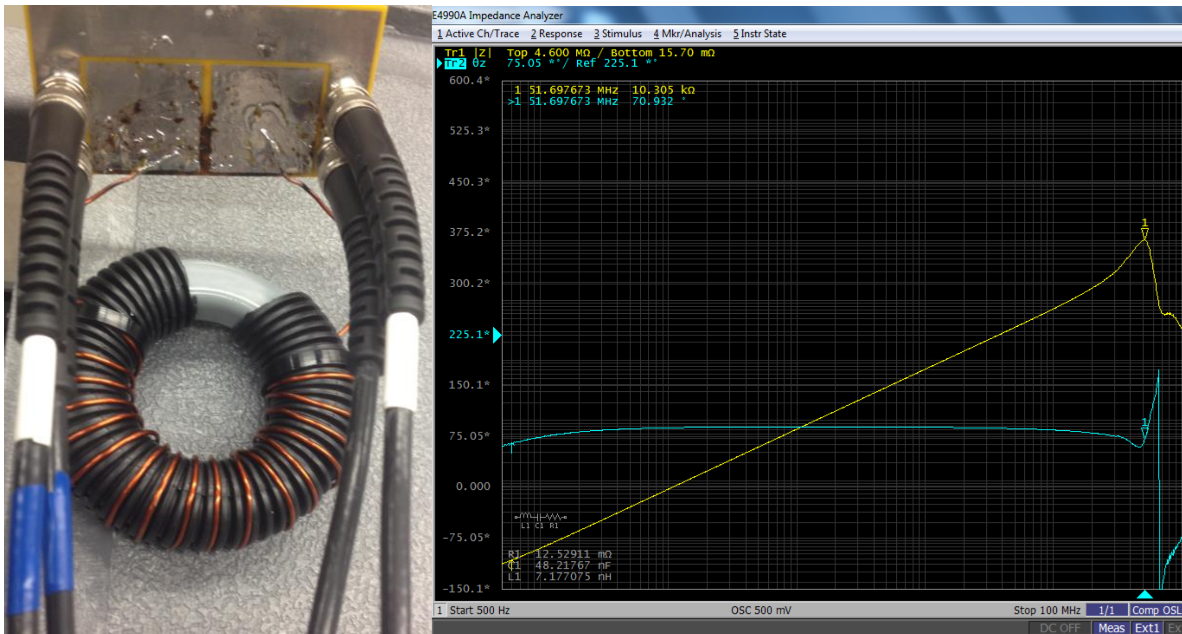
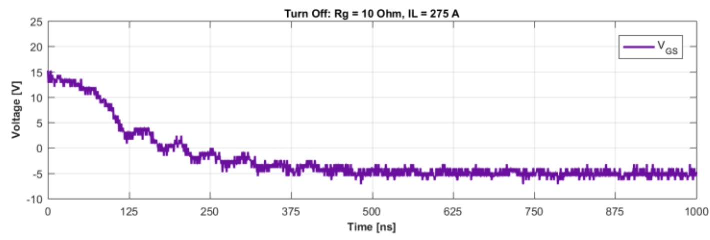
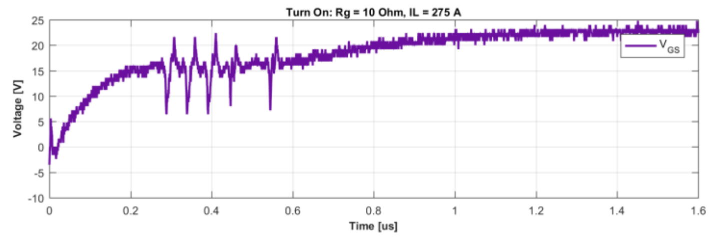


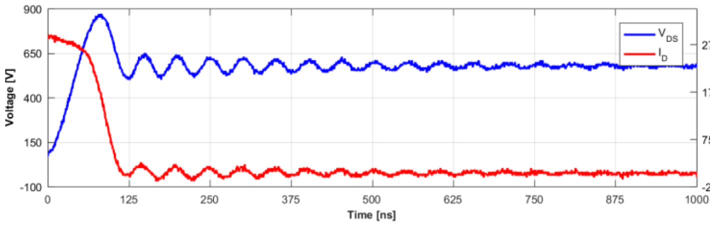
Figure 55: Improved Inductor (a), Frequency Response (b)

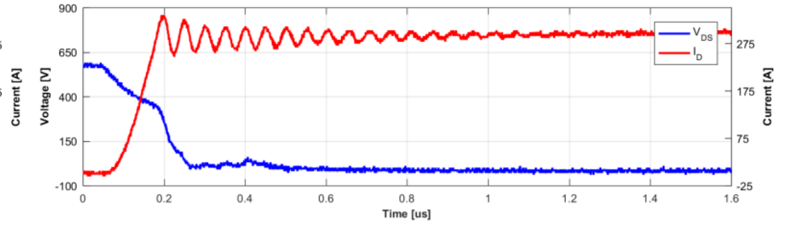
A.2. CIL Results

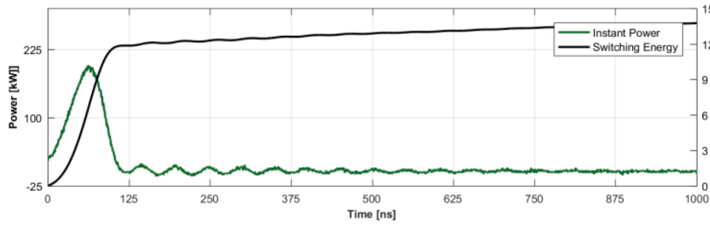
Figure 56 and Figure 57 show additional DPT data collected from the HT-2000. Figure 56 shows the results for 275 A load current and Figure 57 shows the results for 350 A load current. For both, bus voltage is 600 V and the gate resistance is 10 Ω. The conservative gate resistance and high drain current lead to switching losses greater than 10 mJ per switching period. The minimal ringing is also a result of the conservative gate resistance, in conjunction with the high performance load bank. The associated switching losses are presented in Figure 53.











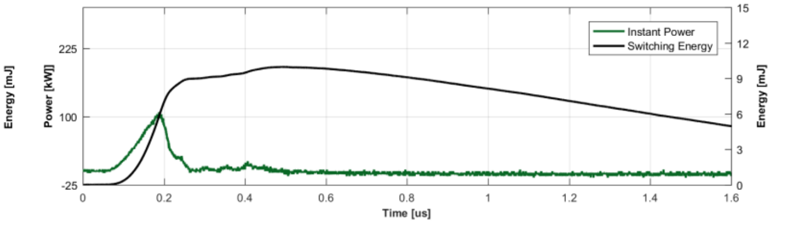
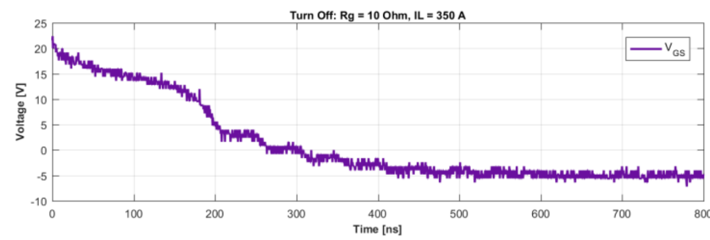
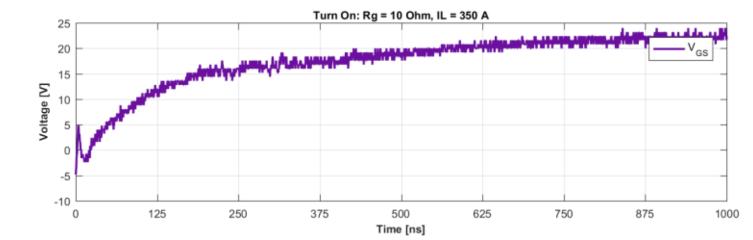
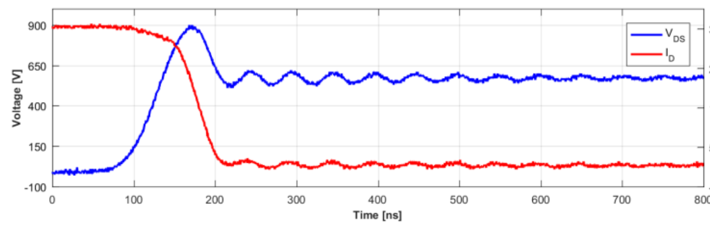
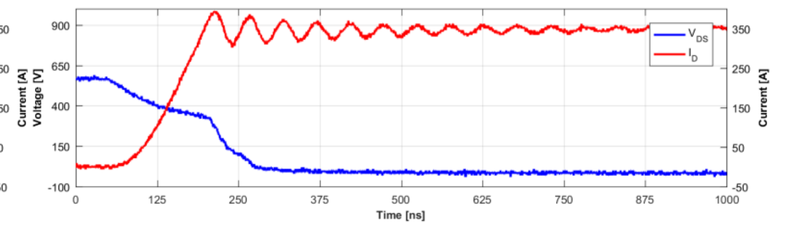


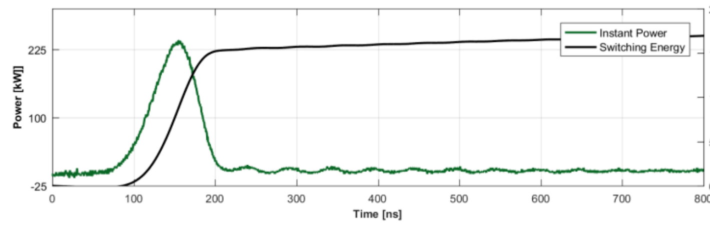
Figure 56: CIL Waveform: 600 V DC bus, 10 Ω Gate Resistor, 275 A Load Current











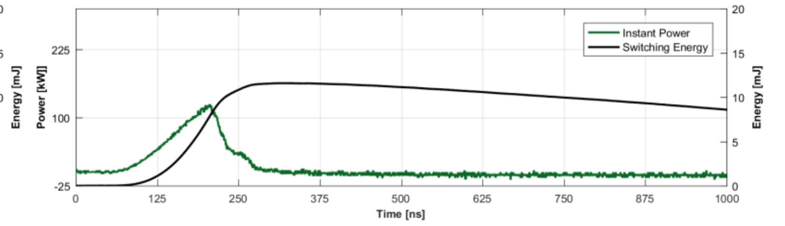


Figure 57: CIL Waveform: 600 V DC bus, 10 Ω Gate Resistor, 350 A Load Current