

ANALYSIS OF LOW VOLTAGE REGULATOR EFFICIENCY
BASED ON FERRITE INDUCTOR

by

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A THESIS

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ABSTRACT

Low voltage regulator based on ferrite inductor, using single- and two-phase topologies, were designed and simulated in MATLAB. Simulated values of output voltage and current were used to evaluate the buck converter (i.e., low voltage regulator) for power efficiency and percentage ripple reduction at frequencies between 1 and 10 MHz with variable loads from 0.024 to 4 Ω . The parameters, such as inductance of 20 nH, quality factor of 15 of fabricated ferrite inductor and DC resistance (DCR) of 8.3 m Ω , were used for efficiency analysis of the converter.

High current around 40 A was achieved by the converter at low load values. Low output voltage in the range of 0.8-1.2 V was achieved. The simulated results for the single- and two-phase converter were compared for maximum efficiency and lowest ripple in output voltage and current. The maximum efficiency of 97 % with load of 0.33 Ω and the lowest ripple current of about 2.3 mA were estimated for the two-phase converter at 10 MHz. In summary, the two-phase converter showed higher efficiency and lower ripple voltage and current than those of the single-phase converter.

In addition, the efficiency of single- and two-phase converters based on ferrite inductor was compared to single- and two-phase converters based on air-core inductor. It was found that the power efficiency of the two-phase converter using ferrite inductor was 10 % higher than the converter using air-core inductor at 10 MHz with a load of 0.024 Ω .

DEDICATION

This thesis is dedicated to my mother, K.Anjani.Devi, for all her love, support and encouragement throughout my life, to my family and close friends who stood by me through the hard times and for giving me constant support.

LIST OF ABBREVIATIONS

DC	Direct current
EMI	Electro-magnetic interference
IC	Integrated circuit
MOSFET	Metal-oxide-semiconductor field-effect transistor
POL	Point-of-load
VRM	Voltage regulator module
CPU	Central processing unit
SPDT	Single-pole double-throw
BJT	Bipolar junction transistor
PWM	Pulse-width modulator
ESR	Equivalent series resistance
DCR	DC resistance
ns	Nano-second
V	Volts
A	Amperes
Ω	Ohms
D	Duty cycle
f_s	Switching frequency
Hz	Hertz
L	Inductance

R	Resistance
Q	Quality factor
CCM	Continuous conduction mode
DCM	Direct conduction mode
RMS	Root mean square
μ	Permeability
ε	Dielectric constant
PCB	Printed circuit board
MMDL	Magnetic Materials and Device Laboratory

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1. INTRODUCTION

1.1 Overview

Low voltage regulators based on ferrite inductor, using single- and two-phase topologies, were designed in MATLAB to evaluate the efficiency, percentage ripple reduction, output voltage and current values. The single- and two-phase converter designs, with buck converter architecture, aimed to achieve a low voltage range of 0.8 V – 1.2 V and currents as high as 40 A. Multiphase topology (i.e., two-phase converter) was designed in order to achieve ripple cancellation and percentage ripple to less than 2 % in the output voltages and currents. To improve the efficiency of the converter, air-core inductor was replaced by ferrite inductor. Efficiency analysis was made on the converters using both inductors at frequency of operation from 1-10 MHz.

1.2 Thesis Outline

Low voltage DC-DC converter has been intensively studied and has developed using certain design techniques, and ferrite inductor is used in the converter. Chapter 1 introduces to the current trends in microprocessors and some of the technical challenges faced by a VRM (voltage regulator modulator) designer. Chapter 2 explains the operation of the basic buck converter and gives supporting equations for calculation of the output values of current, voltage and ripple. Also, the operation of the proposed two-phase converter using uncoupled inductors and equations for calculating the output values of the converter is given. Chapter 3 explains in-depth about the use of ferrite inductors for high frequency applications, the importance of the

parasitic components while modeling the inductor and gives a brief review on various inductor models. Chapter 4 gives the description of the single- and two-phase converter layouts designed in MATLAB using PLECS. Chapter 5 reports the simulated results of the converter and efficiency analysis of the converters. Future work is discussed in Chapter 6.

1.3 Background

The performance of DC-DC converters has been improved significantly over the years. The use of DC-DC converters is increasing in new electronic designs for various applications. Low power devices demand technical requirements, such as accurate and very stable output voltages, excellent load regulation, fast transient response, limited short circuit current, low noise and low electro-magnetic interference (EMI) for their power supplies. Maximum current consumption, current density and current transient of high performance microprocessors have been increasing by 50 % per generation in spite of supply voltage (V_{CC}) scaling [1]. In order to deliver large currents to the microprocessors with high conversion efficiency, without reducing the V_{CC} voltage, voltage regulator and converter modules are used which operate at high frequencies [1]. The demand for high currents with increasing frequency is shown in Fig. 1.

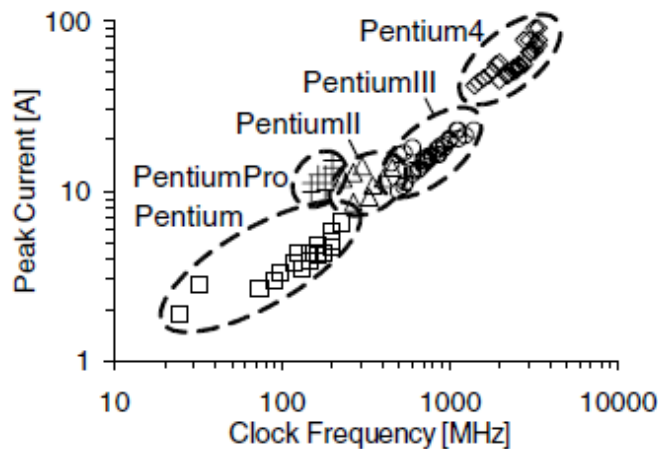


Fig. 1 Increasing peak supply current of high-performance microprocessors [1]

Efficient conversion techniques have been developed to meet these high current requirements for the microprocessors. These techniques have resulted in the subsequent formal growth of an interdisciplinary field of power electronics [2], such as control theory, filter synthesis, signal processing, thermal control, and magnetic components design [3].

For low-end computer systems, such as desktops, workstations and low-end servers, the adopted power delivery architecture is shown in Fig. 2. The silver box provides +5 V and +12 V, which feeds the disk drives and other devices as well as the voltage regulator modules (VRMs). In close proximity to the central processing unit (CPU) or microprocessor (uP), the VRMs step down the voltage to the processor and other integrated circuits (ICs).

Voltage regulation conventionally has been accomplished by linear regulators, but they are slowly being replaced with switching regulators (DC-DC converters). Low voltage, high current and high slew rate for converters are the challenges imposed on power supplies for microprocessors. The centralized silver box, named by Intel, is the typical power source in computer systems. However, with the lower voltage and higher current demands, the parasitic impedance between the centralized silver box and the microprocessor has a severe, negative impact on power quality. Therefore, it is not practical to use the centralized silver box to provide power directly to the microprocessor.

Hence, a point-of-load (POL) regulation system is used to deliver a highly accurate supply voltage to the microprocessor, where a dedicated DC-DC converter, the VRM, is placed

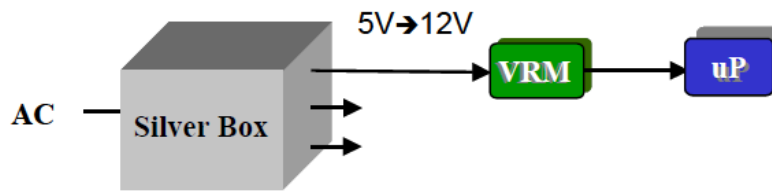


Fig. 2 Power delivery architecture for low-end computer systems

in close proximity to the microprocessor in order to minimize the parasitic impedance between the VRM and the microprocessor [4,5,6,7].

VRMs have been using a single conventional buck or synchronous buck topology for power conversion [8, 9, 10]. They operate at a low switching frequency with a high filter inductance that limits the transient response. This limits the energy transfer speed. In order to meet the supply requirements of the microprocessor, large output filter capacitors and decoupling capacitors are needed to reduce the voltage spike during the transient [11, 12, 13]. Whereas, small output inductance of a multiphase topology increases the energy transfer speed by improving the VRM transient response.

An interleaving approach can reduce the ripple current and increase the ripple frequency, which leads to reduction in output capacitance and improvement in the transient response as well as an increase the VRM efficiency. Interleaving techniques also make it possible to have output inductors of the individual modules in parallel during the transient. Therefore, the effective output inductance can be further reduced, and then, the transient response can be improved.

1.4 Technical challenges of VRM design

To meet future microprocessor supply specifications, high efficiency, high power density and fast transient VRMs are required. To achieve this, the above technology challenges must be addressed and the following potential solutions to these technology challenges have been identified:

- Advanced VRM topologies for high efficiency, high power density and fast transient response to low voltage and high current applications
- Efficient synchronous rectification using new driving means or topologies to eliminate the body diode loss for high-frequency operation
- Innovative integrated magnetics with low core loss, low winding loss and easy manufacturability for high efficiency and high power density
- Optimization of multiphase VRM for the appropriate number of channels and value of output inductance for the optimal design of multiphase VRMs
- Advanced packaging technology to minimize the parasitics for high frequency operation

2. THE BUCK CONVERTER

2.1 Theory of operation of a buck converter

The basic DC-DC *buck converter* using a single-pole double-throw (SPDT) switch, connected to the DC input voltage V_g is shown in Fig. 3. The switch output voltage versus time (t) equals V_g when the switch is in position 1 and is equal to zero when the switch is in position 2 [14].

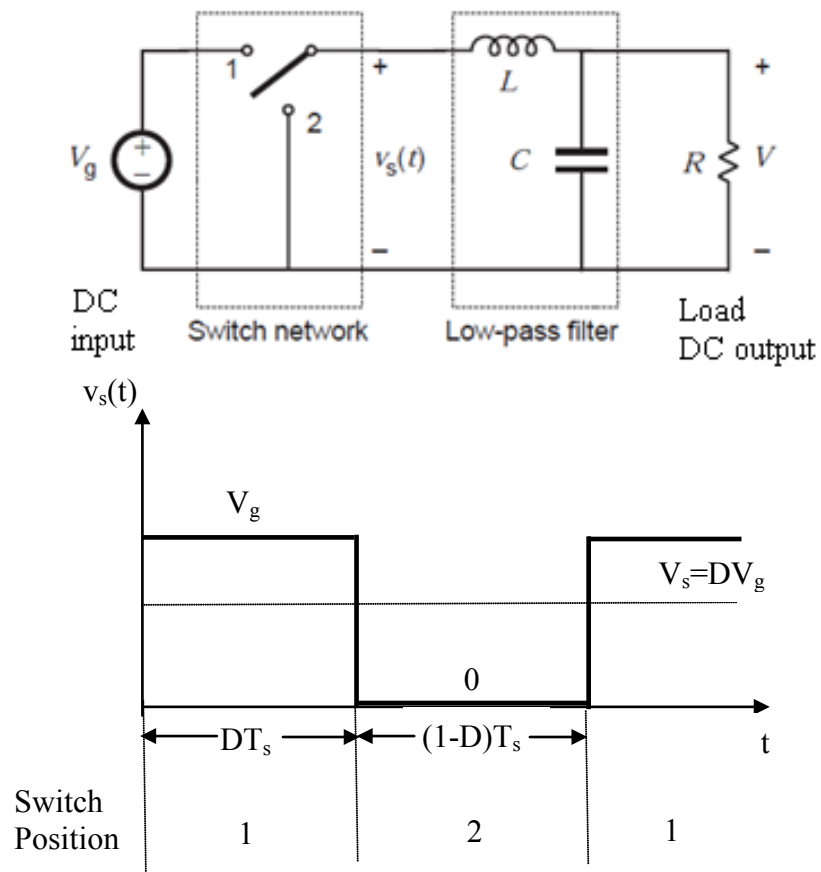


Fig. 3 Simple buck converter and its output voltage waveform [15]

The switch position varies periodically, such that $v_s(t)$ is a rectangular waveform having a period T_s and duty cycle D . The duty cycle is equal to the fraction of time that the switch is connected to position 1, and hence, $0 \leq D \leq 1$. The *switching frequency* f_s equals to $1/T_s$. In practice, the SPDT switch is realized using semiconductor devices such as diodes, power MOSFETs, IGBTs, BJTs, or thyristors. Typical switching frequencies are in the range 1 kHz to 1 MHz depending on the switching speed of the semiconductor device. The switching network changes the DC component of the voltage. By Fourier analysis, the DC component of a waveform is given by its average value. The average value of $v_s(t)$ is given by

$$V_s = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt = DV_g \quad (1)$$

The integral is equal to the area under the waveform or the waveform height V_g multiplied by the duty cycle. It can be seen that the switching network reduces the DC component of the voltage by a factor equal to the duty cycle. Since $0 \leq D \leq 1$, the DC component of V_s is smaller than or equal to V_g .

The power dissipated by the switching network is ideally equal to zero. When the switch contact is closed, the voltage across the contacts is equal to zero, and hence, the power dissipation is zero. When the switch contact is open, there is zero current and the power dissipation is again equal to zero.

Therefore, the ideal switching network is able to change the DC component of voltage without dissipation of power. In addition to the desired DC voltage component V_s , the switch waveform $v_s(t)$ also contains undesired harmonics of the switching frequency. In most

applications, these harmonics must be removed, such that the converter output voltage $v(t)$ is essentially equal to the DC component $V = V_s$. A low-pass filter is employed for this purpose. The converter of Fig. 3 contains a single-stage L - C low-pass filter. The filter has a corner frequency f_o given by

$$f_o = \frac{1}{2\pi\sqrt{LC}} \quad (2)$$

The corner frequency f_o is chosen to be sufficiently less than the switching frequency f_s , so that the filter essentially passes only the DC component of $v_s(t)$. In the case that the inductor and capacitor are ideal, the filter removes the switching harmonics without dissipation of power. Thus, the converter produces a DC output voltage with controllable magnitude via the duty cycle using circuit elements that (ideally) do not dissipate power.

2.2 Basic buck circuit

The buck converter, using a switch network contains power MOSFET and diode as shown in Fig. 4 [14]. A gate drive circuit switches the MOSFET between the conducting (ON) and blocking (OFF) states as commanded by the logic signal $\delta(t)$ in Fig. 4. When $\delta(t)$ is high (for $0 < t < DT_s$), the MOSFET Q_1 conducts current with negligible drain-to-source voltage drop. Hence, $v_s(t)$ is approximately equals to V_g , and the diode is reverse-biased. The positive inductor current $i_L(t)$ flows through the MOSFET. At time $t = DT_s$, $\delta(t)$ becomes low, commanding MOSFET Q_1 to turn off. The inductor current must continue to flow; hence, $i_L(t)$ forward-biases diode D_1 , and $v_s(t)$ is now approximately equal to zero. Provided that the inductor current $i_L(t)$ remains positive, then diode D_1 conducts current for the remainder of the switching period. A diode that operates in the manner is called a *freewheeling diode*.

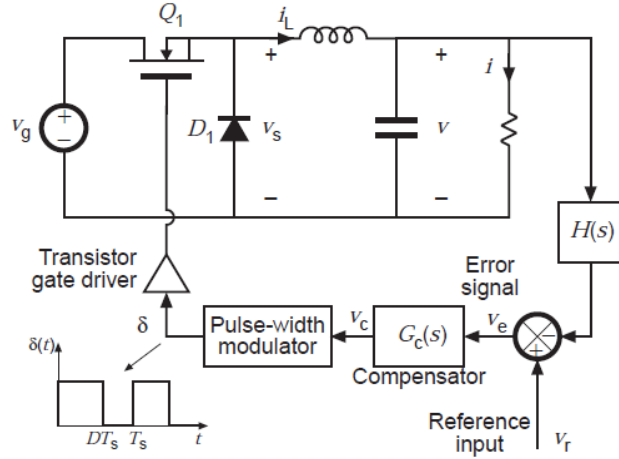


Fig. 4 Buck converter with switch network [15]

Since the converter output voltage $v(t)$ is a function of D , a control system can be constructed that varies the duty cycle to cause the output voltage to follow a given reference voltage v_r . Fig. 4. includes the block diagram of a simple converter feedback system. The output voltage is sensed using a voltage divider and is compared with an accurate DC reference voltage v_r . The resulting error signal is passed through an op-amp compensation network. The analog control voltage $v_c(t)$ is next fed into a *pulse-width modulator*. The modulator produces a switched voltage waveform that controls the gate of the power MOSFET Q_1 . The duty cycle of this waveform is proportional to $v_c(t)$. If this control system is well-designed, then the duty cycle is automatically adjusted such that $v(t)$ follows the reference voltage v_r and is essentially independent of variations in v_g or load current.

2.3 Purpose of different components in the buck converter

In the previous section, the basic switching power supply consists of a few standard components:

- Transistor (active switch)
- Pulse-width modulating controller for operating frequency variation
- Capacitor
- Inductor
- Freewheeling diode (passive switch)
- Feedback circuit

Details on the selection and the functionality of the above components are given below.

Transistor

The transistor is chosen for use in the switching power supply should have fast switching time and must be able to withstand the voltage spikes produced by the inductor. The input on the gate of the transistor is normally a pulse-width modulated (PWM) signal, which will determine the ON and OFF time of the switch. The power switch (transistor) can either be a MOSFET, IGBT, JFET or a BJT. Power MOSFETs are the key elements of high frequency power systems such as high-density power supplies [15]. Therefore, MOSFETs have now replaced BTJ's in new designs operating at much higher frequencies but at lower voltages. At high voltages, MOSFETs still have their limitations. Switching component development aims at minimization of loss by optimizing on-state resistance (R_{ds}) and device charges (for example Q_{gate} and Q_{drain}) [16].

Pulse-width modulating controller for operating frequency variation

The operating frequency determines the performance of the transistor. A PWM controller is generally used to vary the switching frequency. Switching frequency selection is typically determined by efficiency requirements. The higher the switching frequency, the smaller the physical size and component value will be. The reason for this is to reduce even further the overall size of the power supply; this is in-line with miniaturization trends in electronic and computer systems. Therefore, higher frequency reduces the size of the output capacitor.

Capacitor

The capacitor provides filtering by providing a path for redirecting the harmonic currents away from the load. Output capacitance (across the load) is required to minimize the voltage overshoot and ripple present at the output of the step-down converter. The capacitor needs to be large enough so that its voltage does not have any noticeable change during the time that the switch is off. Large overshoots are caused by insufficient output capacitance, and large voltage ripple is caused by insufficient capacitance as well as a high equivalent-series resistance (ESR) in the output capacitor. Since the switching power regulator is usually used in high current, high performance power supplies, the capacitor should be chosen for minimum loss.

Loss in a capacitor occurs because of its internal series resistance and inductance. The capacitor for the switching regulator is partly chosen on the basis of ESR. Solid tantalum capacitors are the best in this respect [17]. The tantalum capacitor is provided with multiple terminals or conductive polymer cathodes [18] to reduce ESR. For high performance power supplies, sometimes it is necessary to connect capacitors in parallel to get a low enough ESR.

Alternative low ESR candidates are polymeric electrolyte and multilayer polymer capacitors [19].

Inductor

The function of the inductor is to limit the current slew rate, which limits the in-rush current through the power switch when the circuit is turned ON. It is noted that the current through the inductor cannot change suddenly. When the current through an inductor tends to fall, the inductor tends to maintain the current by acting as a source. This limits the high-peak current that would be limited otherwise by the switch resistance alone. The key advantage is when the inductor is used to drop voltage, that is, it stores energy. Also, the inductor controls the percent of the ripple and determines whether or not the circuit is operating in the continuous mode.

Peak current through the inductor determines the inductor's required saturation current rating, which in turn dictates the approximate size of the inductor. Saturating the inductor core decreases the converter efficiency, while increasing the temperature of the inductor, the MOSFET and the diode. The size of the inductor and capacitor can be reduced by the implementation of high switching frequency, multiphase interleaved topology, and a fast hysteric controller [20].

A smaller inductor value enables a faster transient response, but it also results in larger current ripple. This causes higher conduction losses in the switches, inductor, and parasitic resistances. The smaller inductor also requires a larger filter capacitor to decrease the output voltage ripple.

The main concern in high frequency inductor design is high magnetic field at windings and fringing fluxes from air gaps. For high efficiency, the conductor should be kept away from the air gap at a distance of 3 times the gap [21], distributed air gap can be used [22] or the gap may be filled with magnetic material [23].

Freewheeling diode and transistor

Since the current in the inductor cannot change suddenly, a path must exist for the inductor current when the switch is OFF (open). This path is provided by the freewheeling diode (or catch diode). The purpose of this diode is not to rectify, but to direct current flow in the circuit and to ensure that there is always a path for the current to flow into the inductor. It is also necessary that this diode should be able to turn off relatively fast. Thus, the diode allows the converter to deliver stored energy in the inductor to the load. This is a reason why we have higher efficiency in a DC-DC converter as compared to a linear regulator. When the switch closes, the current rises linearly. When the switch opens, the freewheeling diode causes a linear decrease in current. At steady state, we have a sawtooth response with an average value of the current.

In many circuits and in the proposed synchronous buck converter of this thesis, the freewheeling diode is replaced by another MOSFET transistor to provide the flywheel function. This arrangement does raise some complications because the buck regulator has to synchronously turn on the flywheel element at just the right times in order to keep the current flowing smoothly. The diode solution turns itself on and off, so it does not require a synchronous

flywheel drive signal. A well-saturated transistor will have a lower voltage drop than the schottky diode, but the diode will help ease and also guarantee the switching transition.

Feedback circuit

Feedback and control circuitry can be carefully nested with the converter to regulate the energy transfer and maintain a constant output to within normal operating conditions. Control by pulse-width modulation is necessary for regulating the output. The transistor is the heart of the switching power supply, and it controls the power supplied to the load.

2.4 Single versus multiphase converters

There are three main limitations of the single-phase buck converter, if employed in applications requiring high current, which are [24]:

- High currents greater than 40 A for notebook, 120 A for desktop and 150 A for server cause excessive I^2R losses, if delivered over one path or phase.
- Processors require low output ripple voltage, while maintaining low output ripple current since $V_{\text{RIPPLE}} = I_{\text{RIPPLE}} * \text{ESR}$. This implies the need for a large inductor because I_{RIPPLE} is proportional to $1/L$.
- The processor power supply must be able to respond quickly to change in power requirement. Unfortunately, the last requirement, fast transient response, implies the need for a small inductor to allow the current through the supply to change quickly, and this conflicts directly with the need for a larger inductor to minimize output voltage ripple.

On the other hand, the uncoupled multiphase buck regulator design resolves these limitations. Instead of using a single high-current path, the multiphase buck converter breaks the current into several lower current parallel paths or phases. Each phase has its own inductor and set of switches, and the current in each phase is summed to form the output current. By activating each phase at a different point in the cycle, the ripple currents of each phase can be overlapped to reduce the overall output current ripple.

2.5 Voltage, current and ripple calculations

Output voltage

Consider the basic circuit of the converter shown in Fig. 5 with resistive load having instantaneous input voltage V_d .

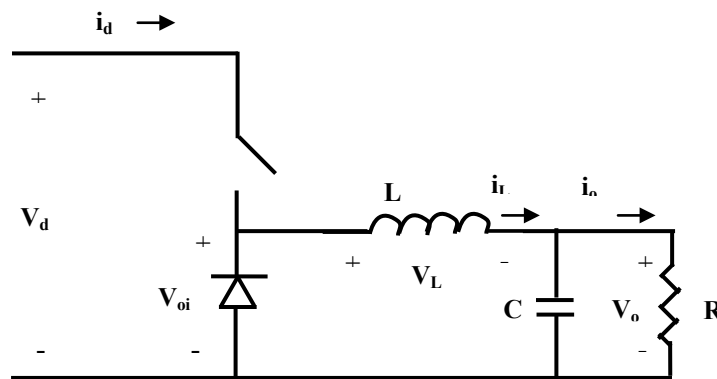


Fig. 5 Basic circuit of buck converter

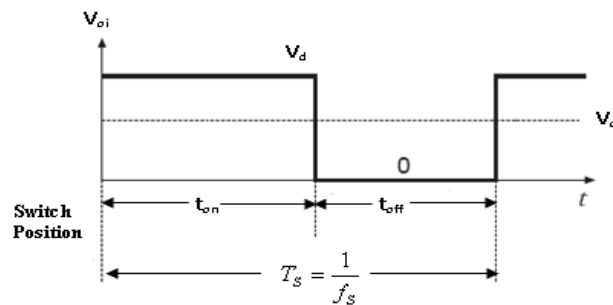


Fig. 6 The output voltage waveform with respect to switch position

The average output voltage can be calculated in terms of duty ratio as:

$$V_o = \frac{1}{T_s} \int_0^{T_s} v_o(t) dt = \frac{1}{T_s} \left(\int_0^{t_{ON}} V_d dt + \int_{t_{ON}}^{T_s} 0 dt \right) = \frac{t_{ON}}{T_s} V_d = DV_d \quad (3)$$

Therefore, V_o can be controlled by t_{ON}/T_s .

The waveform of V_{oi} given in Fig. 6, is the input voltage to the low pass filter, having DC component V_o , with its 1st harmonic at switching frequency f_s and its lower harmonics at multiples of f_s as shown in Fig. 7.

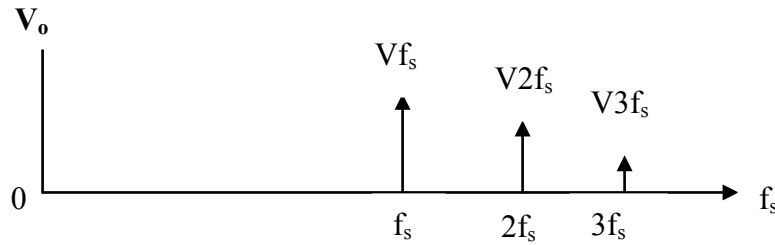


Fig. 7 Output voltage and harmonics at switching frequency f_s

During the ON period of switch, the diode becomes reverse-biased and V_d provides energy to the load and inductor. In the OFF period, the inductor current flows through the diode and transfers some of its energy to the load. The average inductor current is equal to the average output current I_o . Therefore, the average capacitor current in the steady state condition is zero.

Output current

In discontinuous conduction mode, the converter has constant output voltage V_o , this is generally used in the regulated DC power supply; in this case, V_d may change but V_o is kept constant by adjusting D (i.e., $V_d = V_o / D$).

The average inductor current is given as

$$I_{LB} = \frac{T_s V_o}{2L} (1 - D). \quad (4)$$

where $I_{LB} = \frac{1}{2} i_{L,peak} = \frac{T_{ON}}{2L} (V_d - V_o) = \frac{DT_s}{2L} (V_d - V_o) = I_{OB}$.

The maximum value of I_{LB} occurs at $D = 0$ and a constant V_o and is given as

$$I_{LB,max} = \frac{T_s V_o}{2L}. \quad (5)$$

This can be seen in the waveform given in Fig. 8.

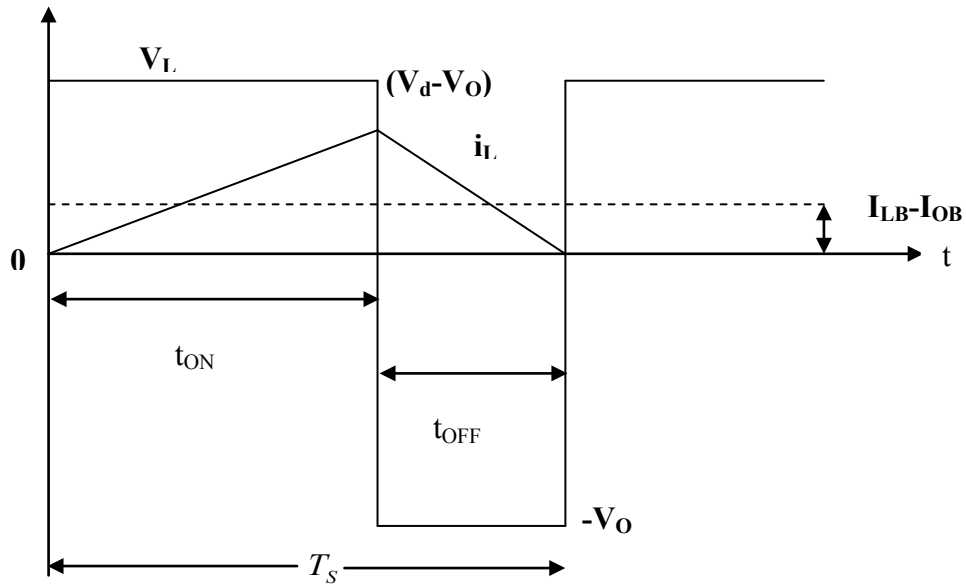


Fig. 8 Output current waveform for ON and OFF periods of the switch

From equations (4) and (5), we obtain $I_{LB} = (1-D) I_{LB,max}$.

The duty ratio in terms of $I_o/I_{LB,max}$ can be given as,

$$D = \frac{V_o}{V_d} \left(\frac{I_o/I_{LB,max}}{1 - V_o/V_d} \right)^{1/2}. \quad (6)$$

Output ripple voltage

The ripple voltage in the output with a practical value of capacitance can be calculated by considering the following wave forms presented in Fig. 9.

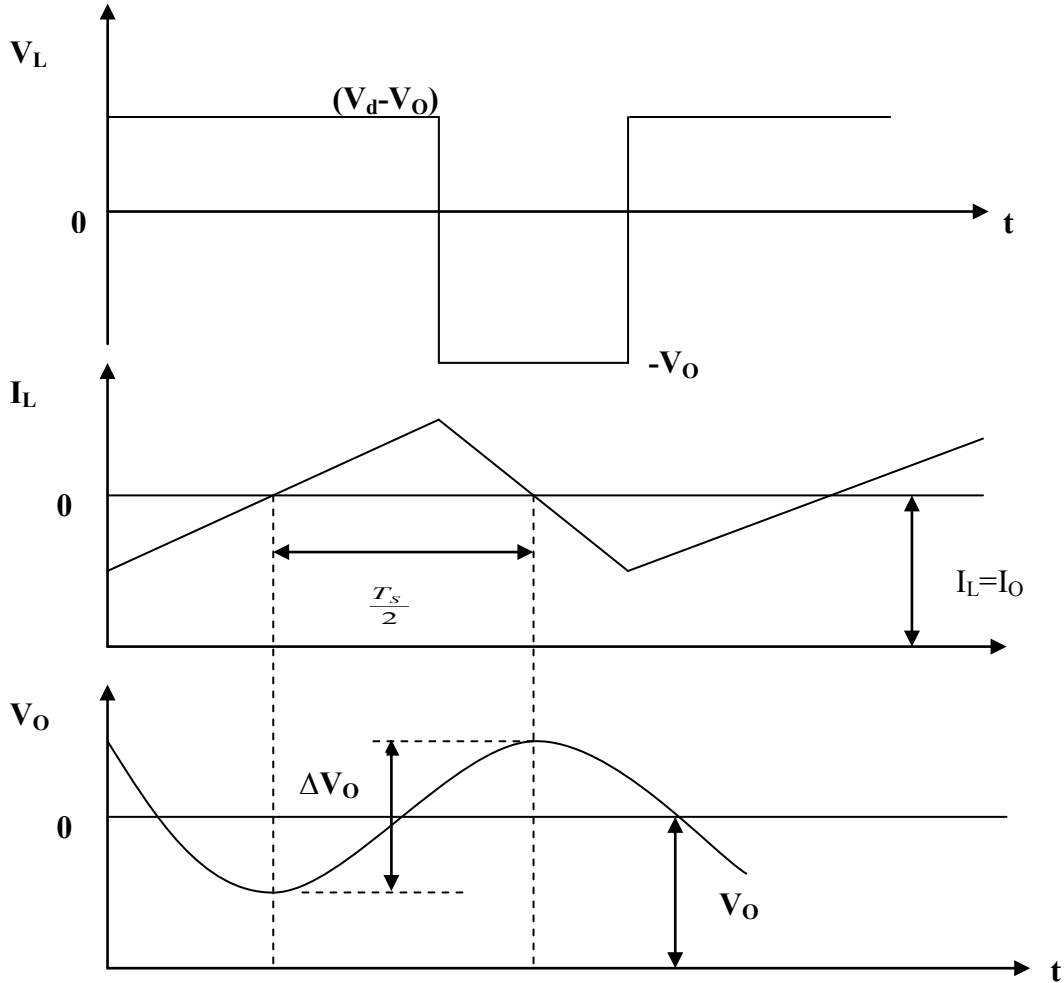


Fig. 9 Output ripple voltage waveforms

This assumes all ripple components of the inductor current i_L flows through the capacitor and its average component goes through the load resistor. Therefore, peak-to-peak ripple voltage becomes

$$\Delta V_o = \frac{\Delta Q}{C} = \frac{1}{2C} \frac{\Delta I_L T_s}{2}. \quad (7)$$

During the t_{OFF} period,

$$\Delta I_L = \frac{V_o}{L} (1-D) T_s. \quad (8)$$

Therefore,

$$\Delta V_o = \frac{T_s}{8C} \frac{V_o}{L} (1-D) T_s \quad (9)$$

and

$$\frac{\Delta V_o}{V_o} = \frac{1}{8} \frac{T_s^2 (1-D)}{2C} = \frac{\pi^2}{2} (1-D) \left(\frac{f_c}{f_s} \right)^2, \quad (10)$$

where $f_s = 1/T_s$ and $f_c = 1/2\pi(LC)^{1/2}$. It is evident that ripple voltage can be reduced, if $f_c \ll f_s$.

2.6 Efficiency considerations

There are some factors that influence the efficiency and the output voltage of the DC-DC converter. The buck converter contains many sources of power dissipation like the series resistance R_{Cin} , parasitic capacitance C_x , stray inductance L_s and the body-drain diodes of power transistors.

The following are a few factors that influence the efficiency of the converter:

- High operating frequency is desired to increase the converter efficiency. The higher the frequency, the smaller the inductance and capacitance. The high frequency induces larger switching loss, gate drive loss, and core loss.
- Efficiency of the converter is dependent on the mode of operation of the switch, namely, CCM (continuous current mode) and DCM (discontinuous current mode).
- Current sharing and current sensing techniques would also influence the overall efficiency of the system (in the case where the current sensing is used to switch between CCM or DCM modes).

Losses in a switch-mode converter can be classified as:

- Load dependent conduction loss (due to transistor ON resistance, inductor winding resistance, and capacitor equivalent series resistance)
- Frequency dependent switching loss (due to transistor and diode output capacitance charge and discharge, gate drive loss, voltage/current overlap at switching transition, inductor core loss, and controller frequency dependent power consumption)
- Fixed loss (due to controller standby current, leakage currents of transistors, diodes, etc.)

These losses are summarized in Table 1 and 2.

Table 1.

Switching loss, gate drive loss and core loss [25]

	CCM	DCM
High Side Switch (PMOS) P_{q1}	$\frac{[I_p^2 + I_p I_v + I_v^2] \times D \times R_{on}}{3}$	$\frac{I_p^2 \times D_1 \times R_{on}}{3}$
Low Side Switch (NMOS) P_{q2}	$\frac{[I_p^2 + I_p I_v + I_v^2] \times (1-D) \times R_{on}}{3}$	$\frac{I_p^2 \times D_1 \times R_{on}}{3}$
Winding Resistance P_{wr}	$\frac{[I_p^2 + I_p I_v + I_v^2] \times R_l}{3}$	$\frac{I_p^2 \times (D_1 + D_2) \times R_l}{3}$
Capacitor ESR P_{esr}	$\frac{1}{3} \left(\frac{I_p - I_v}{2} \right)^2 \times R_c$	$\frac{V_{on} \times R_c \times D_1}{V_o \times I_p} \left[\frac{I_o^3 + (I_p - I_o)^3}{3} + I_p I_o \left(\frac{I_p}{2} - I_o \right) \right]$
Sensing Resistor P_{sen}	$\frac{[I_p^2 + I_p I_v + I_v^2] \times (1-D) \times R_s}{3}$	$\frac{I_p^2 \times D_2 \times R_s}{3}$

R_{on} = ON resistance of MOSFET

R_l = winding resistance

R_c = equivalent series resistance of the capacitor

R_s = sensing resistance

I_p = peak current

I_v = valley current

The duration of high side MOSFET D_1 is:

$$D_1 = I_p L \times f_s / (V_{in} - V_o)$$

The duration of low side MOSFET D_2 is:

$$D_2 = I_p \times L \times f_s / V_o$$

Table 2

Conduction losses [25]

	CCM	DCM
Capacitive Turn ON: $P_{\text{turn-on}}$	$\frac{2}{3}(C_{\text{oss}_p} + C_{\text{oss}_n})V_{\text{in}}^2 \cdot f_s$	$\frac{2}{3}(C_{\text{oss}_p} \cdot (V_{\text{in}} - V_o)^2 + C_{\text{oss}_n} \cdot V_{\text{in}}^2)V_{\text{in}}^2 \cdot f_s$
Turn off Overlapping: P_{over}	$\frac{1}{4}V_{\text{in}} \cdot (I_p \cdot t_{f-p} + I_v \cdot t_{f-n}) \cdot f_s$	$\frac{1}{4}V_{\text{in}} \cdot I_p \cdot t_{f-p} \cdot f_s$
Gate Drive Loss: P_{gate}	$(C_{\text{iss}_p} + C_{\text{iss}_n}) \cdot V_{\text{gs}}^2 \cdot f_s$	$(C_{\text{iss}_p} + C_{\text{iss}_n}) \cdot V_{\text{gs}}^2 \cdot f_s$
Core Loss: P_{core}	$k \cdot I_p^2 \cdot f_s$	$k \cdot I_p^2 \cdot f_s$

where:

C_{oss_p} = high side P-MOSFET C_{oss} (output capacitance)

t_{f-p} = turn off time of high side P-MOSFET

C_{oss_n} = low side N-MOSFET C_{oss} (output capacitance)

t_{f-n} = turn off time of low side N-MOSFET

C_{iss} = input capacitance

In the CCM mode, the switching frequency stays constant, that is $f_s = V_o/V_{\text{in}} \times t_{\text{ON}}$.

The inductor current peak-to-peak value is

$$I_{p-p} = (V_{\text{in}} - V_o) \times V_o / (f \times L \times V_{\text{in}}). \quad (11)$$

The inductor current peak value is

$$I_p = I_o + I_{p-p}/2. \quad (12)$$

The inductor current valley value is

$$I_v = I_o - I_{p-p}/2. \quad (13)$$

In the DCM mode, the switching frequency is proportional to the load, that is

$$f_s = \frac{2 \cdot L \cdot V_o}{t_{on}^2 \cdot V_g \cdot (V_g - V_o)} \cdot I_o. \quad (14)$$

The two tables show the conduction, switching, gate drive and core losses. The total power loss is

$$P_{loss} = P_{q1} + P_{q2} + P_{esr} + P_{wr} + P_{sen} + P_{over} + P_{ptum-on} + P_{core} + P_1. \quad (15)$$

The converter efficiency is

$$\eta(f_s, L, I_{load}) = \frac{P_{load}}{P_{load} + P_{loss}}. \quad (16)$$

2.7 Mode of operation

In the CCM mode (at heavy load), the converter uses fixed frequency control. In this case, inductance, frequency, and load decide the converter efficiency and also determine the minimum capacitance needed (according to the output voltage ripple requirement).

In the DCM mode (at light load), the converter uses variable frequency control. From the loss analysis, the efficiency is independent of frequency. However, for a low-voltage low-power system, it is difficult to maintain a high efficiency at very light load (DCM condition). At light load, the percentage of the control loss in total loss becomes larger. Variable frequency control can improve the power stage efficiency, but it cannot reduce the control loss.

2.8 Current sharing and sensing

Multiphase converter must share load current to balance thermal stress on each phase, so it is important to address current sensing and sharing. Current sharing control method can achieve steady state current balance with an adequate accuracy. These converters use current sharing loops to maintain appropriate current or power sharing among different converter phases, which also supports reliable and stable operation. The current sharing in the converters depends on sensing techniques. Various current sensing techniques are reported, and their comparison is given in Table 3 [26].

Table 3

Various current sensing techniques

Technique	Advantage	Disadvantage
R_{Sense}	Good accuracy	High power dissipation
R_{DS}	Lossless	Low accuracy
L_{Filter}	Lossless	L value shall be known High number of discrete elements
Sensorless	Lossless	L value shall be known
$I_{Average}$	Lossless	ESR value to be known Considers only average inductor current
Transformer	Lossless	Cost, size Not integrable, no IDC information, not practical
SENSEFET	Lossless Integrable Practical Relatively good accuracy	Special MOSFET's, matching issues, low bandwidth

2.9 Control technique

The control scheme used in converter design is pulse-width modulation (PWM).

The PWM control technique has been briefly described in section 2.1. It employs switching at constant frequency, i.e., $T_s = t_{on} + t_{off}$, where T_s is constant time switching period, and t_{on} and t_{off} represent the time the switch is on and off, respectively. By adjusting the t_{on}/t_{off} ratio, the average output voltage can be controlled. This operation can be represented by the following equation for duty ratio.

$$D = \frac{t_{on}}{T_s} = \frac{V_{out}}{V_{in}} \quad (17)$$

Lower power efficiency for small load is the main drawback of this control scheme. The main advantage is the use a single switching frequency, which makes the level of output ripple highly controllable. Also, high power efficiency at large load, high noise and EMI control due to constant switching frequency are achievable.

2.10 Operation of the proposed design network

The circuit in Fig. 10 represents a multiphase buck converter topology, which is a two-phase topology in this thesis.

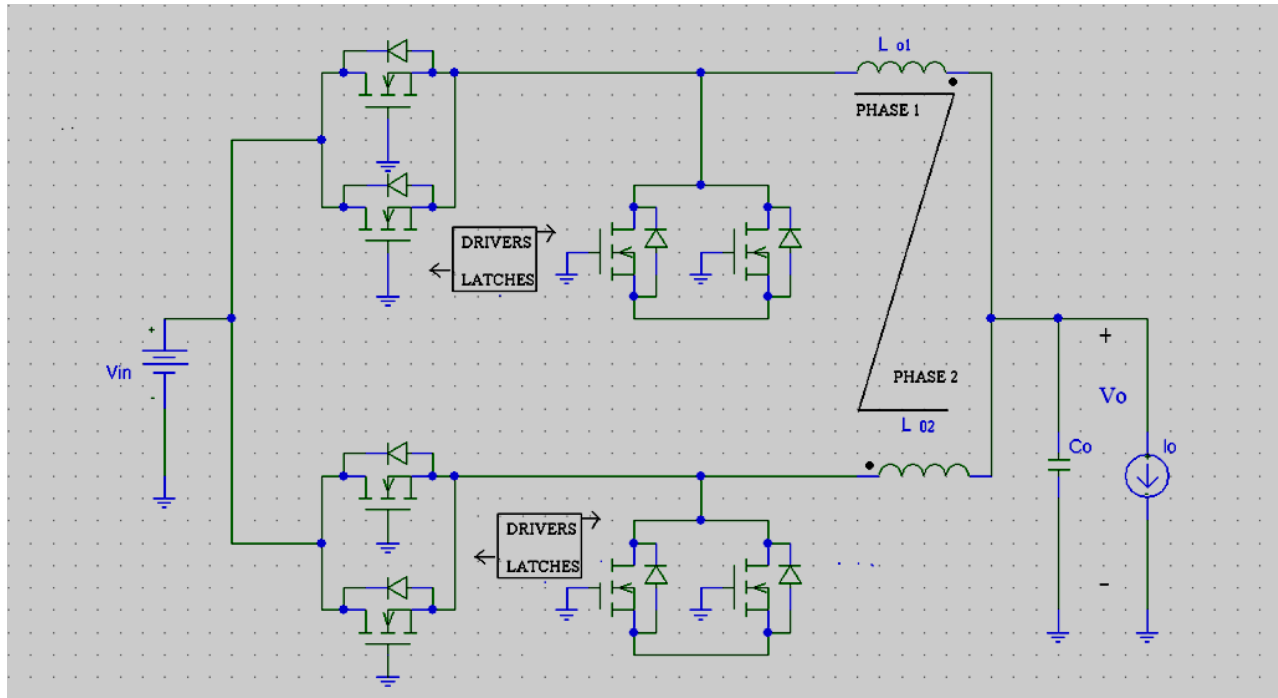


Fig. 10 Multiphase buck converter topology

The limitations of a single-phase buck converter is solved by use of multiphase topology, in other words,

- Reduction of I^2R losses
- Maintaining low output ripple current
- Fast transient response

The MOSFET, which is combined with diodes in parallel acts as switch to the circuit. The simplified circuit having two switches in each phase, switches Sw_1 , Sw_2 , Sw_3 and Sw_4 is shown in Fig. 11.

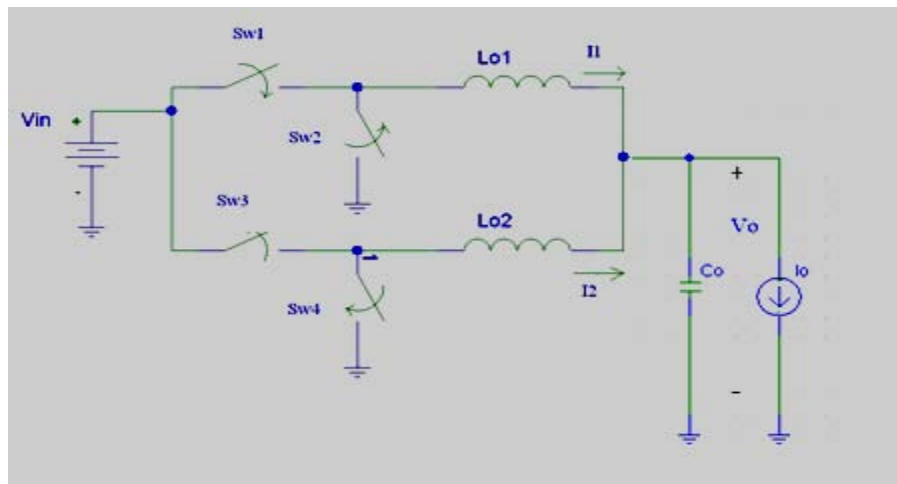


Fig. 11 Simplified buck converter topology

Operation of the converter studied in this thesis is described as follows.

The latches and drivers can have the following 4 states:

1. Sw_1 and Sw_4 ---> ON (Sw_2 , Sw_3 OFF) (presented in Fig. 12)
2. Sw_2 and Sw_4 ---> ON (Sw_1 , Sw_3 OFF) (presented in Fig. 13)
3. Sw_3 and Sw_2 ---> ON (Sw_1 , Sw_4 OFF) (presented in Fig. 14)
4. Sw_1 and Sw_3 ---> ON (Sw_2 , Sw_4 OFF) (presented in Fig. 15)

First consider State 1 (Sw₁ and Sw₄ ---> ON (Sw₂, Sw₃ OFF)), which is presented in Fig. 12.

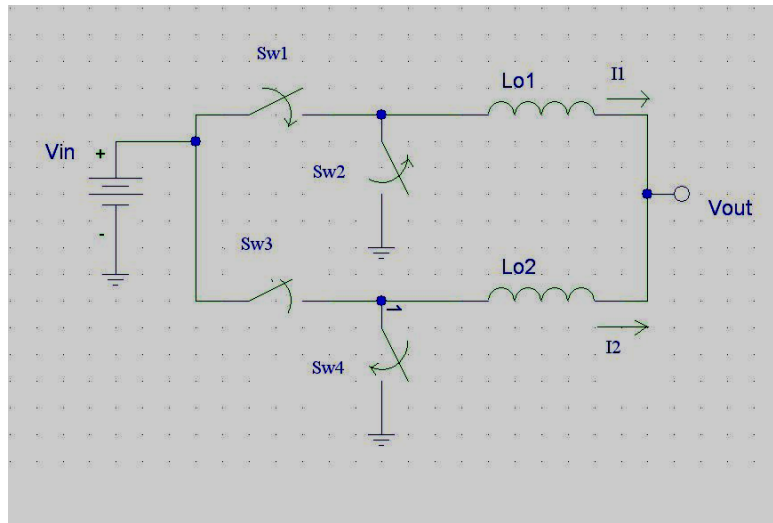


Fig. 12 Operation of two-phase converter in State 1

The duration of ON time is from $t = 0$ to $t = DT_s$. The buck converter has output voltage as $V_{OUT} = DV_{IN}$.

T_s = Time interval

$f_s = 1/T_s$ = Switching frequency

Voltage across $L_{o1} = V_{IN} - V_{OUT}$

Voltage across $L_{o2} = -V_{OUT}$

According to Faraday's law, $dt = DT_s$.

The current equations, where i_1 is current in L_{o1} and i_2 is current in L_{o2} , can be written as follows.

$$V_{IN} = L_{o1}(1-D) \frac{di_1}{dt} \quad (18)$$

$$V_{IN} = -L_{o2}D \frac{di_2}{dt} \quad (19)$$

Rearranging the above equations, we get

$$di_1 = (V_{IN}/L_{o1})(1-D)DT_s \quad (20)$$

$$di_2 = (-V_{IN}/L_{o2})(D)DT_s. \quad (21)$$

Therefore, output current is given by

$$I_{OUT} = I_1 + I_2. \quad (22)$$

Assuming $L_{o1} = L_{o2} = L$,

$$di_{OUT} = di_1 + di_2 = di_1 = V_{IN} L(1-2D)DT_s. \quad (23)$$

From equations (18) and (19), it is noted that in phase 1, L_{o1} is increasing, which means storing energy and in phase 2, L_{o2} is decreasing, which means sourcing energy.

The case of State 2 (Sw_2 and $Sw_4 \rightarrow ON$ ($Sw_1, Sw_3 OFF$)) is shown in Fig. 13.

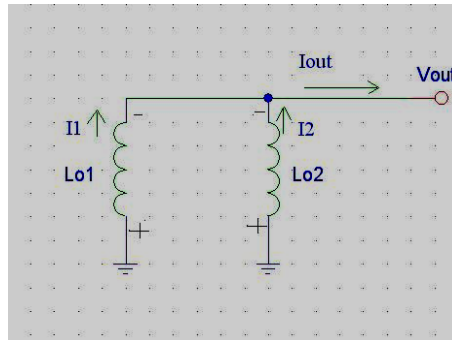


Fig. 13 Operation of two-phase converter in State 2

The time period in this case is from $t = DT_s$ to $t = DT_s/2$ and voltage across both inductors is equal to $-V_{OUT}$.

The current equations can be represented by the following equations.

$$dt = (0.5-D)T_s \quad (24)$$

$$di_1 = (-V_{IN} / L_{o1})(0.5-D)DT_s \quad (25)$$

$$di_2 = (-V_{IN} / L_{o2})(0.5-D)DT_s \quad (26)$$

Output current is given by $I_{OUT} = I_1 + I_2$.

Assuming $L_{o1} = L_{o2} = L$,

$$di_{OUT} = di_1 + di_2 = (-V_{IN} / L)(1-2D)DT_s. \quad (27)$$

During this time period, both the inductors are decreasing in energy as they are sourcing energy to the output.

The case of State 3 (Sw_3 and $Sw_2 \rightarrow ON$ ($Sw_1, Sw_4 OFF$)) is shown in Fig.14.

The time period is from $t = T_s/2$ to $t = T_s/2 + DT_s$.

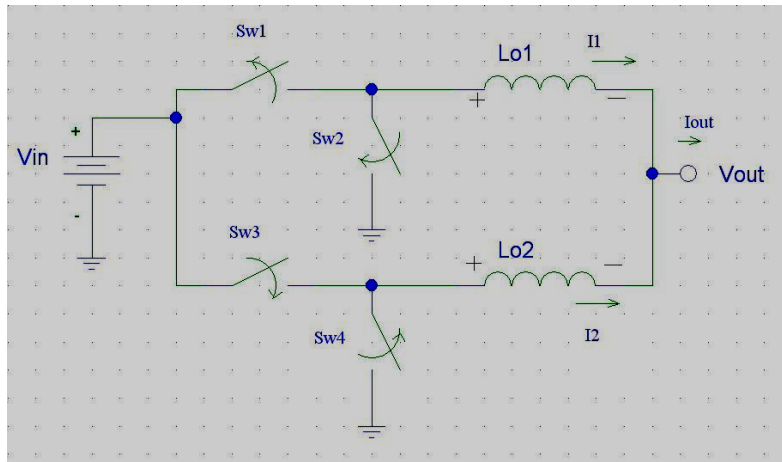


Fig. 14 Operation of two-phase converter in State 3

The current equations are as follows.

$$di_1 = (-V_{IN} / L_{o1})(D)DT_s \quad (28)$$

$$di_2 = (V_{IN} / L_{o2})(1-D)DT_s \quad (29)$$

Output current is given by $I_{OUT}=I_1+I_2$.

Assuming $L_{o1} = L_{o1} = L$,

$$di_{OUT} = di_1+di_2 = di_1 = V_{IN} L(1-2D)DT_s. \quad (30)$$

The case of State 4 (Sw_2 and Sw_4 ---> ON (Sw_1, Sw_3 OFF)) is described in Fig. 15.

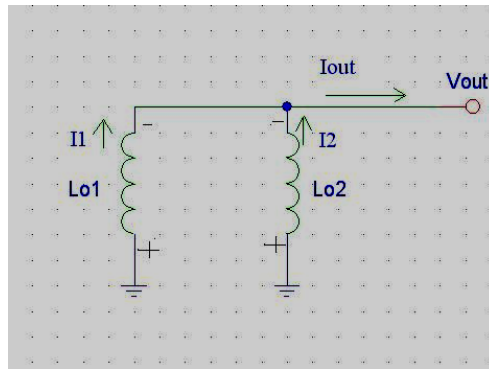


Fig. 15 Operation of two-phase converter in State 4

The current equations can be represented by the following equations.

$$di_1 = (-V_{IN} / L_{o1})(0.5-D) \quad (31)$$

$$di_2 = (-V_{IN} / L_{o2})(0.5-D)DT_s \quad (32)$$

Output current is given by $I_{OUT} = I_1+I_2$.

Assuming $L_{o1} = L_{o1} = L$,

$$di_{OUT} = di_1+di_2 = (-V_{IN} / L)(1-2D)DT_s. \quad (33)$$

From above equations, it is noted that the output currents are increasing in States 1 and 3 and are decreasing in States 2 and 4, and this cycle keeps repeating. The output current ripple occurs at twice the switching frequency and phase ripple occurs at $1/T_s$.

For uncoupled two-phase buck converter, current equations are given as (when $L_{o1}=L_{o2}=L$)

$$di_1 = di_2 = (-V_{IN}/L)(1-D) DT_s \quad (34)$$

$$di_{OUT} = (-V_{IN}/L)(1-2D) DT_s. \quad (35)$$

The above case is given for uncoupled inductors in the two-phase buck converter, which meets the power requirements by maintaining minimum output voltage ripple (is proportional to di_{OUT}) and allowing the use of smaller inductance per phase for fast transient response. However, inductance per phase in uncoupled buck converter decreases the ripple current and increases the di per phase. This increases peak current per phase and the switching losses and I^2R losses, which also affects the overall efficiency of the power supply.

The voltage and current ripple percentages are calculated by using the equations given below:

$$\%V_{ripple} = \frac{\delta V_o}{V_o} \times 100 \quad (36)$$

$$\%I_{ripple} = \frac{\delta I_o}{I_o} \times 100 \quad (37)$$

Whereas, the power efficiency of the converter is calculated by,

$$\%Efficiency = \frac{Output\ Power}{Input\ Power} = \frac{V_o I_o}{V_i I_i} . \quad (38)$$

3. MODELING CONSIDERATIONS FOR INDUCTOR

3.1 Introduction

High switching frequency is becoming essential to achieve designs that are required for next generation handheld electronics. The reduction in size of handheld electronic hardware demands a low voltage operation and high output current. The main unit in portables devices responsible for such functionality is the DC-DC converter. For this reason, the converter should maintain high efficiency in order to achieve a longer battery life, while compressing it to fit on a smaller silicon die. The inductor occupies the largest area in a DC-DC converter. Different ideas of integrating the inductor on-chip are proposed to achieve a miniaturized DC-DC converter, which operates at high frequencies.

One advantage of high frequency operation is reduction in the inductor size, which results in a lower turns ratio, consequently, reducing resistive losses. The main problem with a smaller inductor is that the average RMS current of the transistor switch will increase. As a result, there is an increase in the conduction losses. This is because the peak current rating of the inductor will increase, which in turn would require the use of large capacitors at the output.

3.2 Ferrite inductors

Power inductor designs have led to successful point-of-load (POL) modules (DC-DC converters), which meet the demands of low profile, high power surface mount inductors with current ratings up to 25 A. The basic core material used is iron for the inductor design.

Other alloys and oxide formulations of iron improve the core material characteristics. It is important to select the core material for minimizing the power losses. The DC current can saturate the inductor fast in the absence of air gap in the core's magnetic path. For a design with constraints on current saturation level, a high flux ferrite or soft metal alloy is a good choice. Also, the ferrite material's saturation level decreases as the operating temperatures increases; whereas in the case of soft iron alloy, the saturation level does not decrease.

The high resistive nature of ferrite materials allows them to operate more efficiently at higher frequencies. Changes in flux density, frequency or temperature vary the core losses in the material. New ferrite and soft iron alloy will provide new solutions to meet the challenge for small size in footprint and height as well as higher current-handling capability of the DC-DC converters.

Buck converters are commonly used in low power devices that use integrated or external passive components for the LC output filter. High operating frequencies of the converter leads to reduction in the inductor size with a low inductance value capable for integration. As described before, the inductor's performance and efficiency are affected not only by the choice of the core materials, but also by the geometrical parameters of the inductor.

3.3 Inductor modeling

To have an accurate physical model, it is necessary to identify the parasitics and their effects on the inductor design. A simple extraction procedure is followed to characterize the inductor. The scattering parameters (S -parameters) are obtained using a vector network analyzer,

these parameters are converted to corresponding admittance parameters (Y -parameters). L , R and Q are then calculated using the relations given in Appendix A.

An equivalent circuit model of an inductor is shown in Fig. 16 [27].

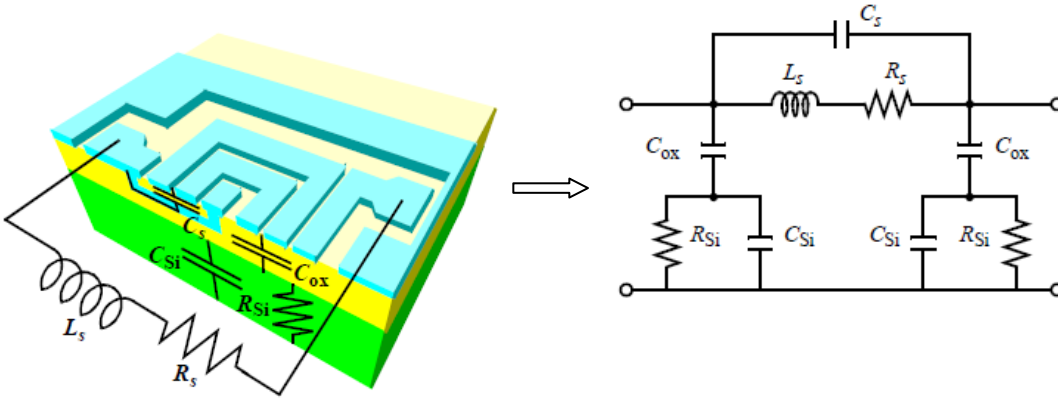


Fig. 16 Physical model of a magnetic inductor and its equivalent circuit model [27]

3.4 Review on ferrite inductors for DC-DC converter applications

Planar inductor on thick magnetic substrate was developed to show that the presence of magnetic substrate enhances the inductance (L) up to 100 % for μ (permeability) $\gg 1$, and for large values of μ , L becomes independent (inductance enhances by factor of $2\mu/(\mu+1)$). Also, the permeability and thickness of the ferrite substrate complement each other for enhancement of inductance [28]. It was suggested in [29] that Ni-Zn ferrites as substrate materials should be used for maximum enhancement of the inductance. They have small permeabilities ($\mu = 100$) and smaller dielectric constants ($\epsilon = 10$, to give smaller distributed parasitic capacitances). Increase in L increases quality factor (Q).

Another planar inductor with circular spiral pattern was developed for operating at few hundreds of kilo-hertz switching in DC-DC converter. The design of the inductor was based on

parameters of coil line/space (d/p ratio = 0.875), magnetic properties of magnetic sheets (relative permeability $\cong 4000$, saturation magnetization $\cong 6700$ G and almost zero magnetostriction) to ensure large inductance, low resistance loss and high quality factor Q [30]. It was observed that the inductance was constant (about 30 μH) up to 1 MHz and the maximum quality factor was 11 at about 150 kHz. The DC coil resistance was about 0.65 Ω and Q was estimated to be 30 at 150 kHz [30]. This inductor was tested in a converter at 250 kHz, which gave an output of 5 V and 2 W, with 1.7 W/cc. It was also proven that the inductance was scarcely dependent on external size of the inductor for frequency > 1 MHz, which leads to miniaturization of thin-film inductors for MHz switching converters.

An investigation on Q_{max} with respect to frequency shows that Q_{max} appears where iron loss (core hysteresis loss plus core eddy current loss) and copper loss (conductor DC loss) are equal [31]. Reduction in copper loss increases Q_{max} , but it occurs at low frequency, and while low iron loss increases Q_{max} , it occurs at higher frequency.

The planar inductor with meander coil in Fig. 17 is embedded in magnetic (NiZn) plates with a narrow air-gap for uniform distribution of magnetic flux and to reduce iron loss. This inductor is applicable for a 10 W-class power capacity buck converter operating at 2 MHz with 82 % efficiency [32]. A new structure of double rectangular spiral coil is embedded in CoZrNb thin film to allow rotational magnetization. The inductor shows an inductance 1 μH (up to 10 MHz), Q of 10 at 10 MHz and was tested in a switching chopper DC-DC converter to achieve output power of 5 W at 5 MHz operating frequency [33]. A similar structure is shown in Fig. 18 was fabricated using FeBN magnetic films, in which inductor shows inductance of 1 μH and Q

of 4 up to 5 MHz, and it was implemented in a buck converter whose output power was 1.5 W with 300 mA of current. The efficiency of 80% was achieved at 1.8 MHz [33].

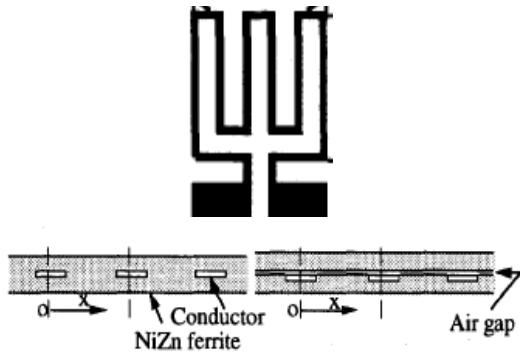


Fig. 17 Meander coil pattern, its cross sectional spiral sandwich type and views of inductors without air gap and with air gap [32]

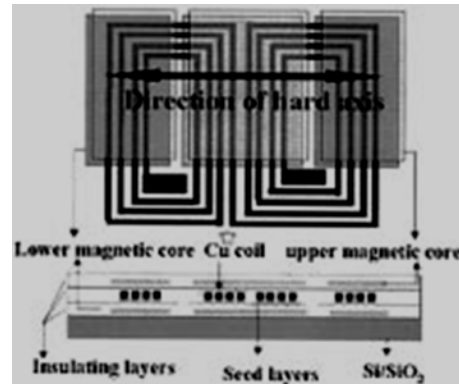


Fig. 18 Schematic diagram of a dual magnetic thin film inductor [33]

Furthermore, a one-turn inductor having V-groove in Fig. 19 filled with different core materials of Co-Zr-O, Fe-Al-O and Co-Fe-B-Si-O, was fabricated to study the tradeoff between saturation flux density and resistivity in soft magnetic materials. Efficiency in the range of 80 to 90 % in a 3.3 V to 1.1 V buck converter with 7 A output current was achieved [34]. The selection of the material was based on power density which was chosen for the type of application.

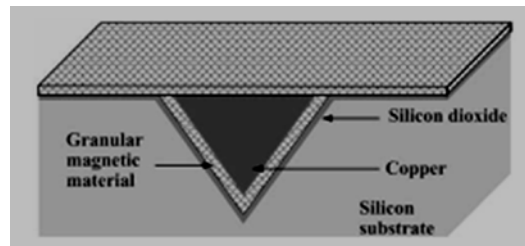


Fig. 19 Schematic of V-groove inductor (not to scale) [34]

A planar inductor with two-turn Cu coil which is embedded in Ni-Zn ferrite substrate and top layer of Fe composite (40 % Mn-Zn) of relative permeability 6 was fabricated to constitute in a synchronous buck converter. The converter achieved a conversion efficiency of 80 % at 4 A with switching frequency of 1 MHz [36]. A maximum Q of 30 at 4 MHz was observed, and the inductance was found to decrease with increasing frequency and was 4 times that of air core inductor.

Also, PCB (printed circuit board) integrated inductor for low power converter was fabricated. This inductor shows 4.7 μH of inductance, 500 mA maximum current [37] and 0.81 μH of inductance with 45 of Q at 10 MHz, 470 mA of DC current, with small size profile of 4.5 mm \times 5.5 mm \times 0.5 mm (height) [38]. An integrated micro-fabricated inductor with 440 nH of inductance and 11.7 of Q at 5.5 MHz and conversion efficiency of 92 % was also achieved in a converter [39].

3.5 Summary

The use of ferrite inductor improves the performance and efficiency of DC-DC converters as compared to those using air-core inductor. At high frequency of operation, it is possible to miniaturize the inductor by tailoring of geometrical parameters and magnetic properties of the core material. Inductance is low, in range of nano-Henries, at high frequency (>1 GHz), but it is required to have high Q value to meet the low voltage, high current and high efficiency requirements for future DC-DC converters.

4. DESCRIPTION OF THE CONVERTER LAYOUTS IN MATLAB

To meet the future voltage and current requirements for DC-DC converters in microprocessors and portable devices (given in Appendix B), a single-phase open loop buck converter and a two-phase open loop buck converter were proposed and evaluated. MATLAB along with PLECS was used to simulate these designs. Efficiency analysis was performed on the converters using ferrite and air core inductors, operating at frequencies ranging from 1 MHz to 10 MHz (note: Efficiency analysis was performed excluding the AC losses and switching losses). Theoretical and simulated values were compared and were in good agreement with each other.

4.1 Description of the designed converters

- The models were designed to test the efficiency of a single- and two-phase converter of variable frequencies and load.
- Inductor of 20 nH inductance value with equivalent DCR of air-core and ferrite core inductors, respectively, were used.
- ESR value for the capacitor considered was as low as 0.1 m Ω .
- The output resistive load was varied between 0.024 – 4 Ω to obtain output current values of 200 mA to 50 A and output voltage around 0.8 V to 1.2 V (step down from 3.5 V input).
- The buck converter is an open loop model with no feedback control. The control is given externally by the PWM with a set constant duty cycle.

4.2 Single-phase open loop converter layout in MATLAB

The single-phase converter was designed in MATLAB, using PLECS module, as seen in Fig. 21. The diode of the conventional buck converter was replaced with MOSFET for this design. To make the converter work as a synchronous rectifier, both the upper and lower side ideal switches are used in the PLECS circuit (given in Appendix C) and each switch has ON resistance of $3\text{ m}\Omega$ (R_{DS_ON}). Use of ideal switches avoids the need for introducing delay between the ON and OFF times of the MOSFET switches. The driver block generates alternating pulses for the upper and lower MOSFET switches.

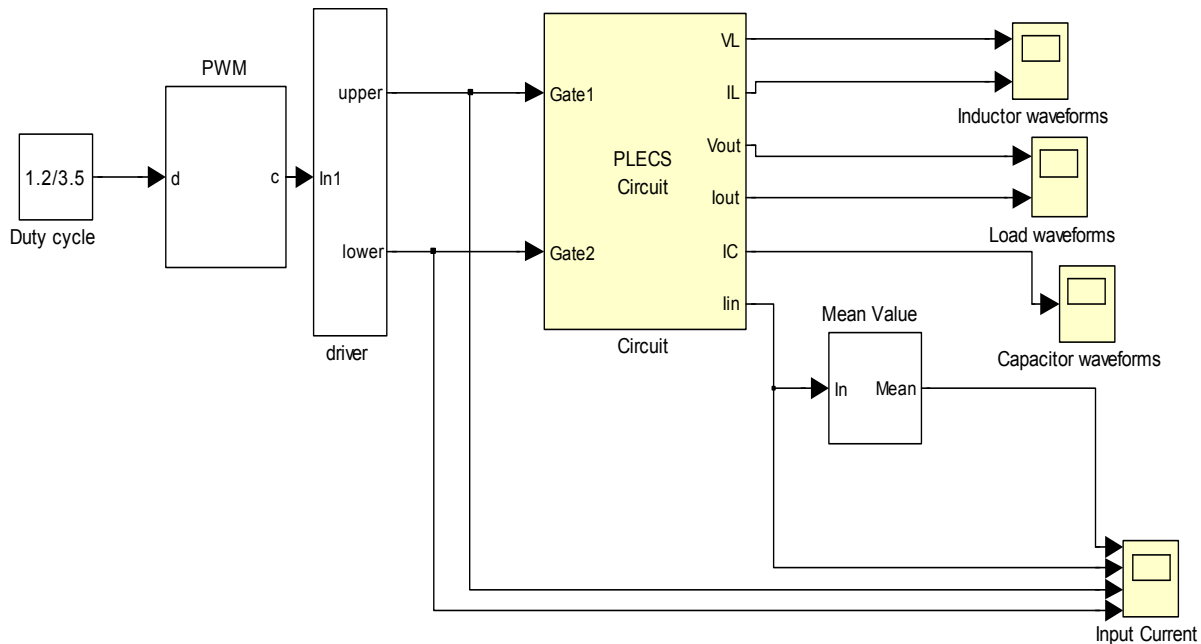


Fig. 20 Single-phase converter layout designed in MATLAB using PLECS module

The converter was operated at different frequencies and using variable loads. The equations in Chapter 2 were used to calculate the theoretical values of output voltage, current and ripple voltages using MATHCAD (given in Appendix C).

4.3 Two-phase open loop converter layout in MATLAB

The two-phase converter, designed in MATLAB using PLECS module, is shown in Fig. 21. The design has the same parameters for the components used in the single-phase converter design. As mentioned previously, the two-phase converter was designed with aim at ripple cancellation, faster transient response and current sharing and 180 degree change between the phases.

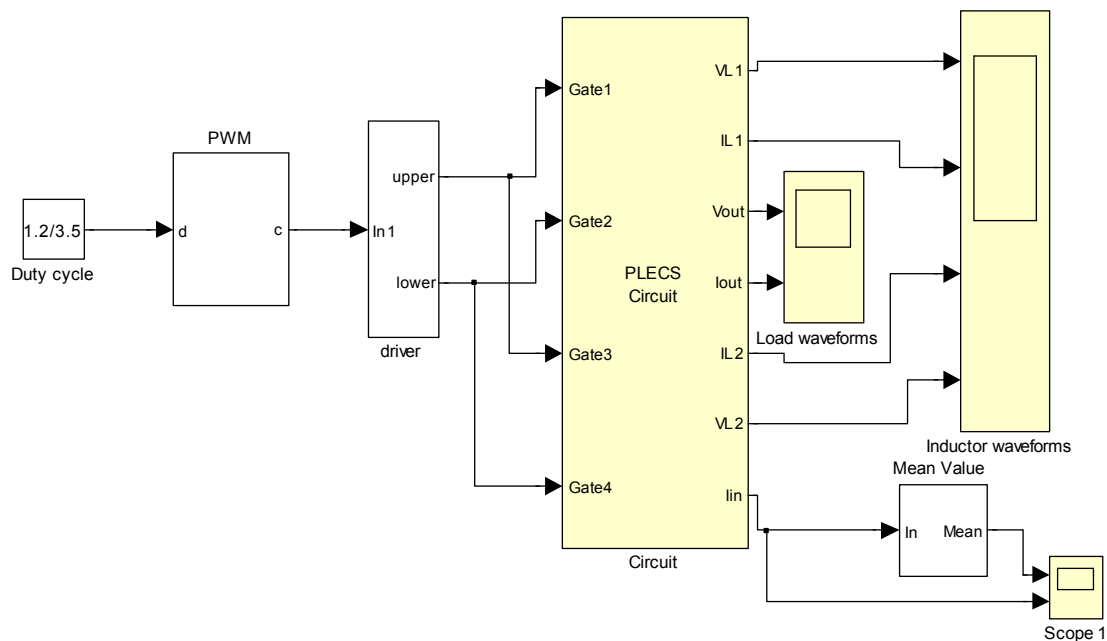


Fig. 21 Two-phase converter layout designed in MATLAB using PLECS module

This design was also operated at different frequencies and variable loads for the efficiency analysis.

Table 4

Specifications of the converter

Input Voltage, V_{in} (V)	3.5 V
Output Voltage, V_{out} (V)	0.8 ~ 1.2 V
Load Current, I_o (A)	1~ 50 A
Frequencies of Operation (Hz)	1, 5, 10 MHz
Duty Cycle, $D (V_{out}/V_{in})$ %	34 %
Inductance, L (nH)	20 nH
Capacitance, C (uF)	~ 560 uF
MOSFET Resistance (R_{dson})	3 m Ω

1. RESULTS AND DISCUSSION

The simulated output voltage, output current and inductor current waveforms for the single- and two-phase buck converter are shown Fig. 23 and 24, respectively. Fig. 24 gives the inductor waveforms for the two inductors used in the two-phase converter, which show that current is shared between the two-phases of the buck converter with equal inductance values.

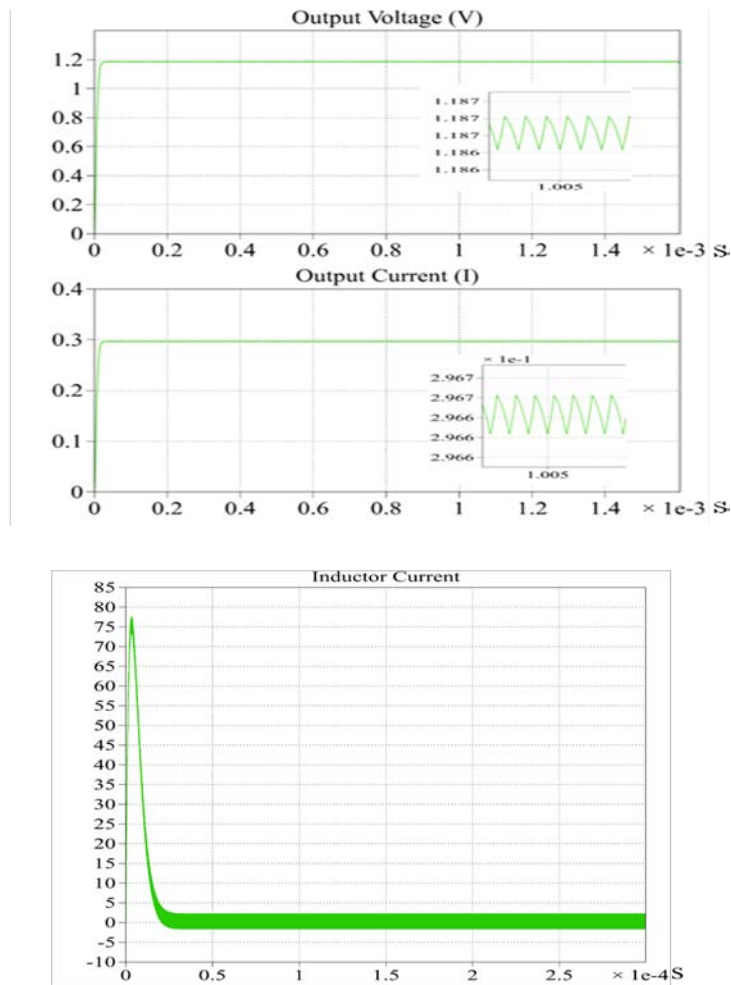


Fig. 22 Simulated output voltage, output current and inductor current waveforms of single-phase converter

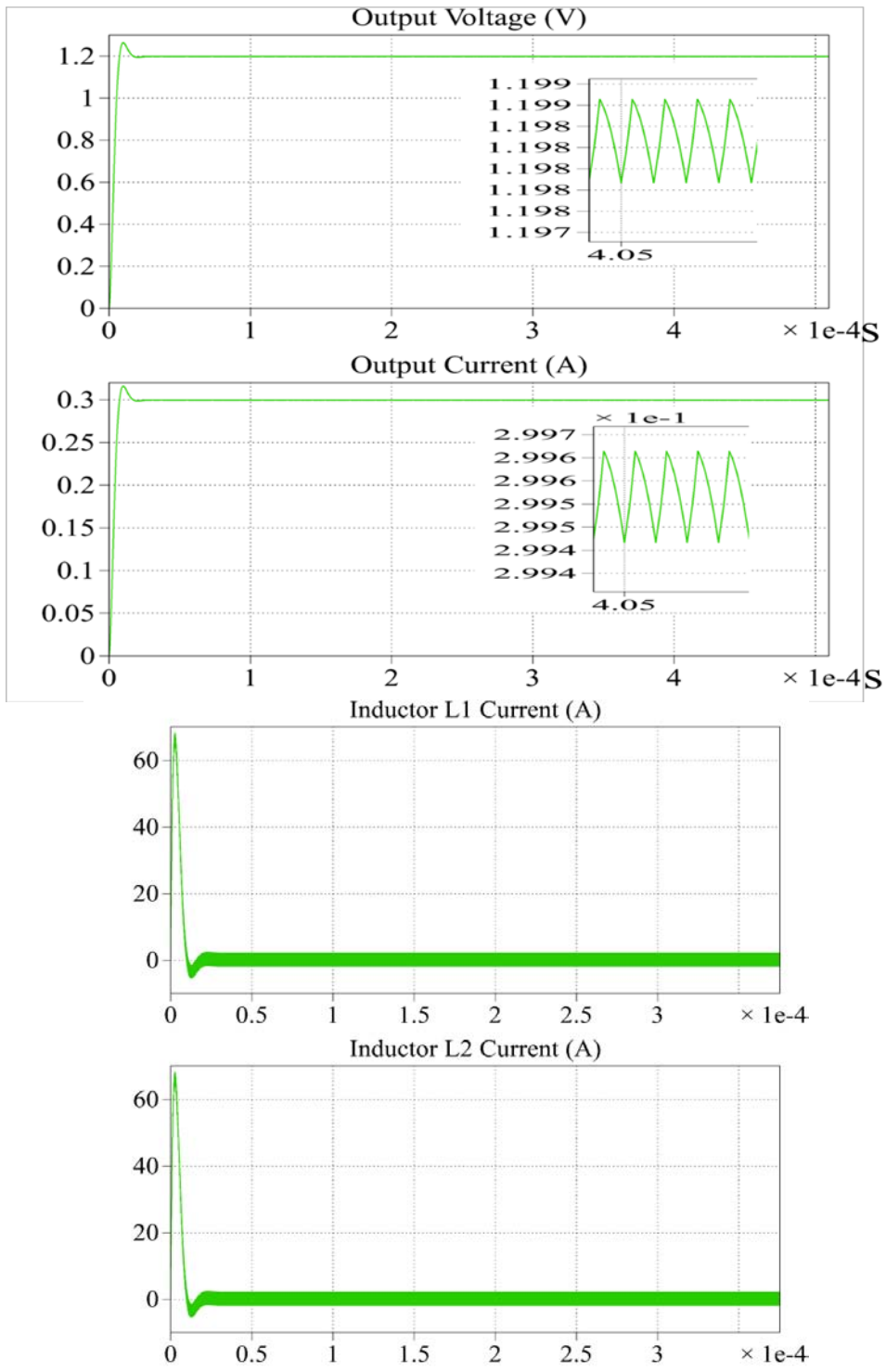


Fig. 23 Simulated output voltage, output current and inductor current waveforms of two-phase converter

Analysis was done on the converter using the ferrite inductor. For the single- and two-phase converter, percentage efficiency was plotted at different frequencies of operation (1, 5, and 10 MHz) with different load conditions as shown in Fig. 24. The efficiencies of air-core inductor of 20 nH with DCR = 0.01 Ω were compared with the ferrite inductor of 20 nH with DCR = 0.0083 Ω . DCR value of air-core inductor was taken from [40]. The DCR of the ferrite inductor was extracted from the simulated data of L and Q at 10 MHz [41].

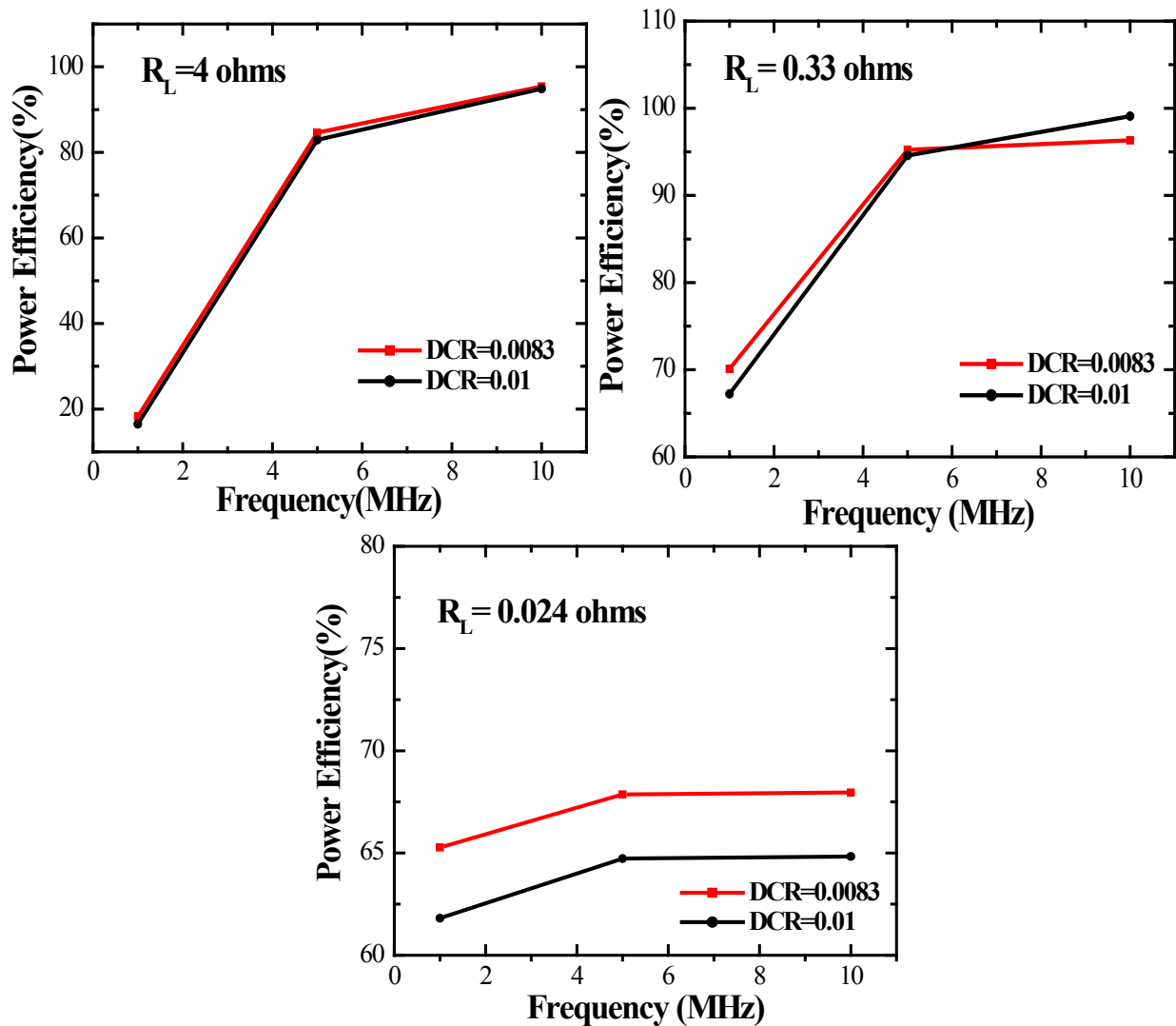


Fig. 24 Power efficiency versus frequency of single-phase converter for $R_L = 4, 0.33, 0.024 \Omega$

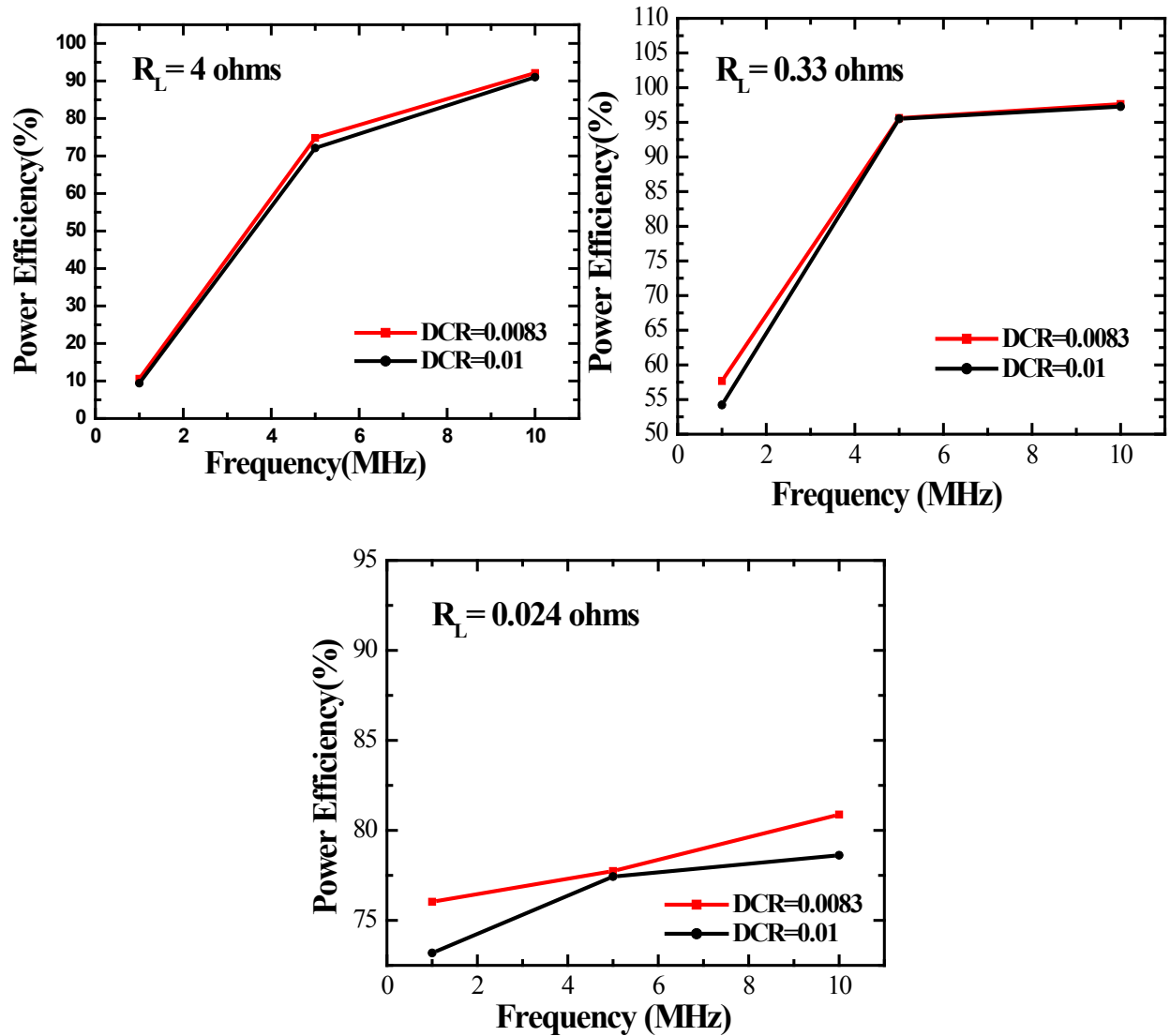


Fig. 25 Power efficiency versus frequency of two-phase converter for $R_L = 4, 0.33, 0.024 \Omega$

It is observed from the plots that power efficiency of the converters has been improved when ferrite inductor is used compared to air-core inductor due to its lower DCR. In Fig. 25 when $R_L = 4 \Omega$, the efficiency values were higher for $DCR = 0.0083 \Omega$ than $DCR = 0.01 \Omega$ over the same range of frequencies. This shows that the higher value of DC resistance contributes to power loss in the inductor, and hence, reduces the efficiency of the converter (note: the parasitic capacitances were neglected in this model). Also, when the load is $R_L = 0.024 \Omega$, the efficiency of

the converter based on ferrite inductor is higher than that of air-core inductor as shown in Fig. 25. The two-phase converter efficiency was higher than the single-phase converter, when $R_L = 0.024 \Omega$, at 5 MHz. The efficiency of the single-phase converter is 67.87 % whereas for the two-phase converter an efficiency of 77.74 % was observed. For the same load, single-phase converter showed an efficiency of 67.79 %, and the two-phase converter showed 80.88 % at 10 MHz operating frequency. This proves that the multiphase converter improves the efficiency of the DC-DC converter and efficiency also increases with increase in frequency. With more number of phases, an improvement in efficiency is observed. However, as the number of phases increase, the circuitry becomes complex and the number of inductors increases. This will increase the size of the converter. One solution to this is integrating the inductor in the converter.

The efficiencies of the single- and two-phase converters based on the ferrite inductor were compared for variable loads over the range of frequencies from 1-10 MHz as seen in Fig.26(a) and (b).

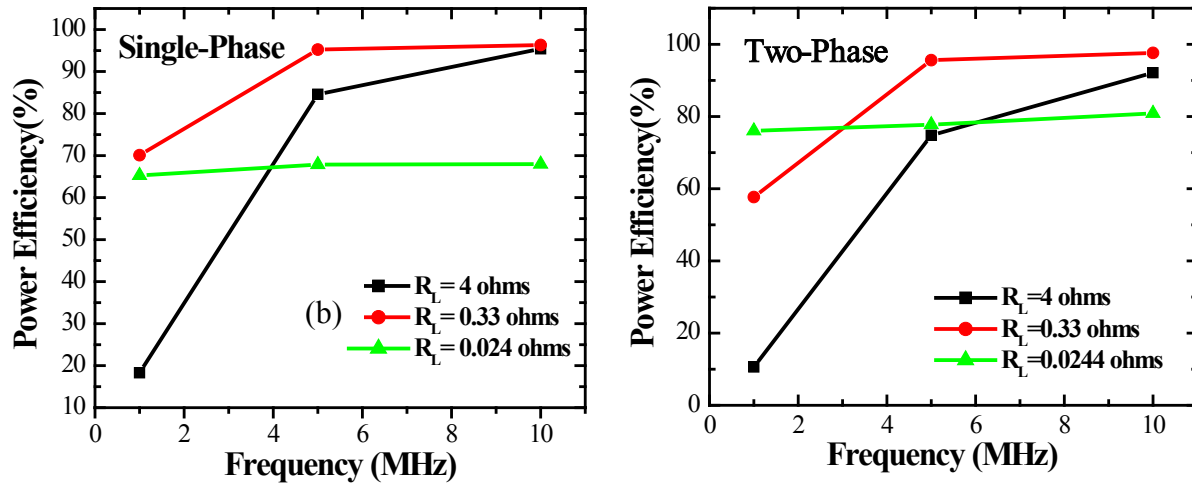


Fig. 26 Efficiency versus frequency for (a) single-phase converter and (b) two-phase converter based on ferrite inductor with variable loads

It is seen that as the load increases, the efficiency of the converter (single- and two-phase) varies. In Fig. 26(a), the efficiency of the single-phase converter, when $R_L = 0.024 \Omega$, $R_L = 0.33 \Omega$, and $R_L = 4 \Omega$, is 67.96 %, 96.32 % and 95.4 % at 10 MHz, respectively. In case of the two-phase converter at 10 MHz frequency, when $R_L = 0.024 \Omega$, the efficiency is 78.62 %, while the efficiency is 97.27 % and 91 % when $R_L = 0.33 \Omega$ and $R_L = 4 \Omega$, respectively, as seen in Fig. 26(b).

The lower efficiency values for variable loads is contributed to the load dependent conduction losses such as the transistor ON resistance, diode forward voltage drop, inductor winding resistance (DCR) and capacitor equivalent series resistance (ESR). At high load condition, most of the power loss comes from the conduction losses, and at light load conditions, the gate drive and switching losses cause the power loss in the converter which reduces the overall efficiency of the DC-DC converter.

The voltage and current variations for the single- and two-phase converters for variable loads is shown in Fig. 27.

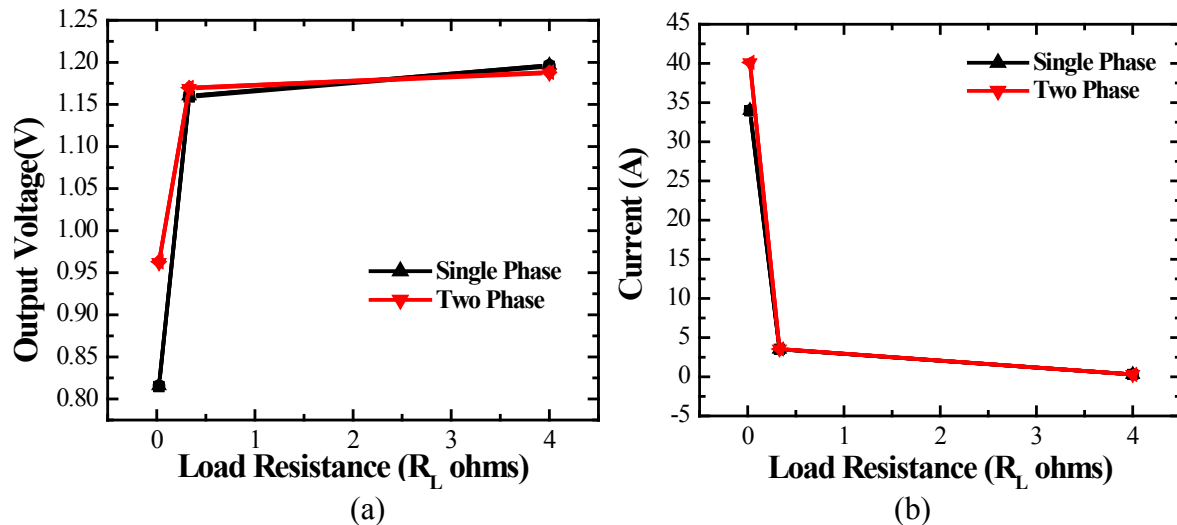


Fig. 27 (a) Output voltage versus load resistance for single- and two- phase converter and (b) output current versus load resistance for single- and two-phase converter

In Fig. 27(a), it is seen that low voltages were achievable from 0.8 to 1.2 V for increasing load resistances using a 20 nH ferrite inductor in the DC-DC converter for the frequency range of 1 MHz-10 MHz. The voltage values for the single- and two-phase converter were close. In Fig. 27(a), when $R_L = 4 \Omega$ and at 10 MHz frequency, V_{out} for the single-phase converter was 1.195 V and 1.187 V for the two-phase converter.

Fig. 27(b) shows that for lower loads, high currents in the range of 30 A to 45 A can be obtainable; these currents are suitable for microprocessor applications. For light loads, the two-phase converter gave higher output current than that of the single-phase converter. Accordingly, when $R_L = 0.024 \Omega$, the output current I_{out} for the single-phase converter was 33.9 A, and for two-phase converter, it was observed to be 41.1 A. It is evident from this that the multiphase converter provides high currents compared to that of conventional converters. Also, as the load increases, the output current is reduced and reaches hundreds of milli-amperes, which can be made suitable for portable applications.

The percentage current ripple versus frequency is shown in Fig. 28.

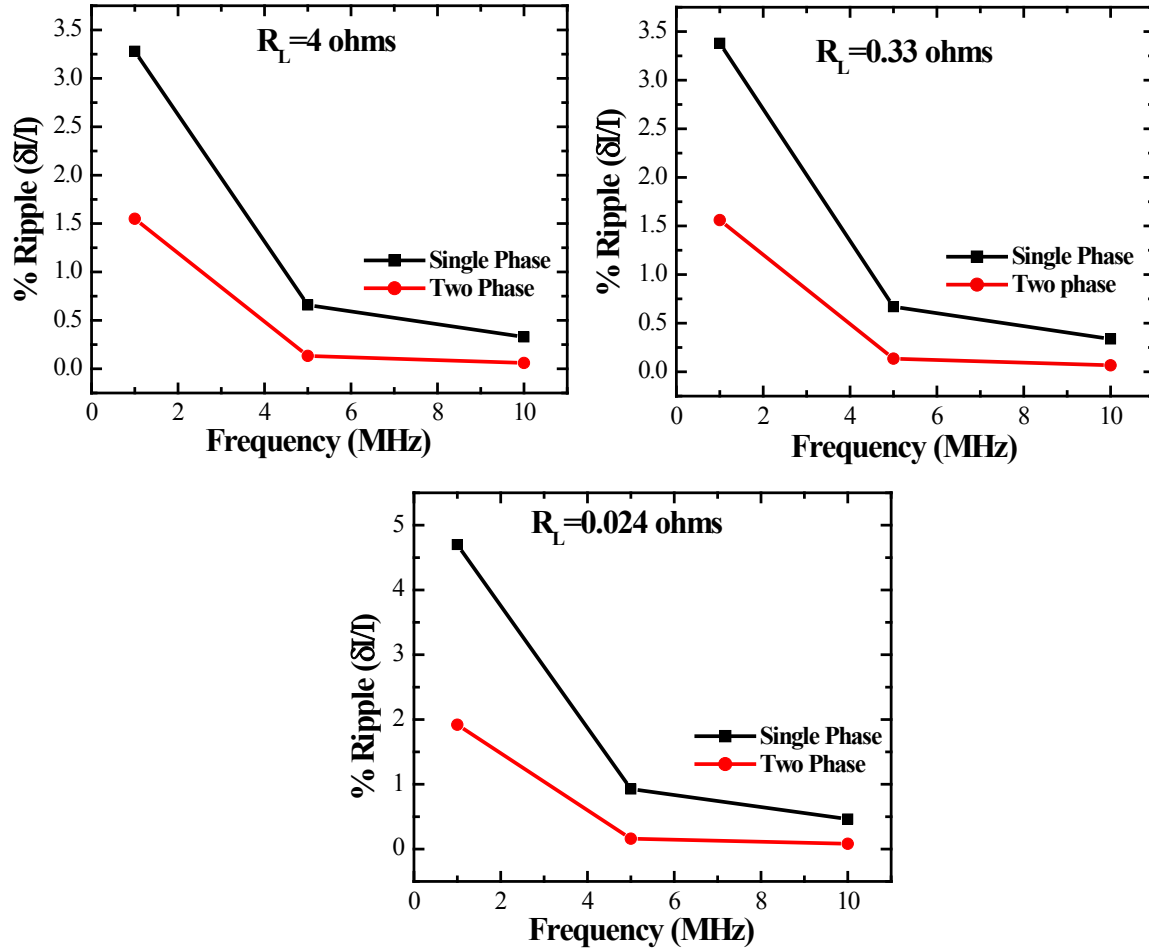


Fig. 28 % Ripple ($\delta I/I$) versus frequency for single- and two-phase converter for various frequencies

The percentage output ripple was dramatically reduced with increase in frequency. Less than 2 % of percentage current ripple was achievable. When compared to the single-phase converter, high ripple reduction was observed in a two-phase converter for all load conditions over the studied range of frequencies (1 MHz-10 MHz). In Fig. 28(k), when $R_L = 4 \Omega$ and at 10 MHz, the percentage output ripple current was 0.32 % for the single-phase converter and 0.081 % for the two-phase converter. The lowest ripple current value of 0.1 mA was obtained at 10

MHz with $R_L = 4 \Omega$ for the two-phase converter. Also, the output ripple voltage showed similar behavior.

This shows that the increase in the number of phases of the converters helped in ripple reduction as there is ripple cancellation between the phases of the converters. Thus, the two-phase converters helps in achieving lower percentage of ripple compared to single-phase converters at increasing frequencies of operation.

6. CONCLUSION AND FUTURE WORK

A single- and two-phase DC-DC buck converter was designed and simulated in MATLAB (using PLECS module) for testing the converter performance using a ferrite inductor with 20 nH inductance and a quality factor of 15. Higher efficiencies (up to 97 % at 10 MHz) of converter using equivalent model parameters of ferrite inductor were achieved when compared to air-core inductors (which have high DCR that of ferrite inductor). Also, efficiency was improved with increase of the frequency.

Low voltage (0.8 V to 1.2 V) and high currents (up to ~ 40 A) were achieved for variable loads. The two-phase converter provided higher current outputs than the single-phase converter at low loads. Output ripple reduction as low as 0.06 % at 10 MHz was achieved.

Future work would include adding a feedback loop to the converter design to regulate the output voltage. The feedback system needs to be designed to provide a high bandwidth control loop, which would reduce the output capacitors for use in multiphase converters. Design of multiphase (more than two phases) converters which consider the coupling effect of the ferrite inductors is needed to improve the efficiency of the DC-DC converters and would potentially meet the voltage and current requirements for application to future microprocessors and portable devices.

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APPENDIX

APPENDIX A

Parameters extraction for physical model of inductor

There are various ways to integrate magnetic materials into the inductor structure, one of which is shown below in Fig. a.

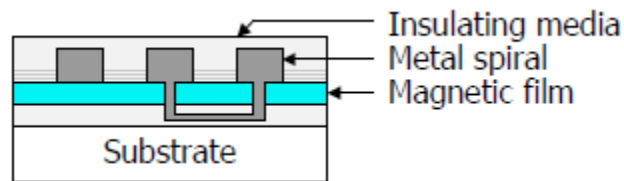


Fig. a Physical model of magnetic inductor

When magnetic thin-films are added under the inductors, the lumped-element model is modified, as seen in Fig. b, where L_m , R_{loss} , C_m , R_m , R_{mc} , and C_{mlap} are added. L_m represents the inductance contribution of magnetic material to the metal spiral caused by the real part of the relative permeability (μ_r') of the magnetic thin-film. R_{loss} expresses the magnetic loss in the magnetic thin-film due to the imaginary part of permeability (μ_r'') of μ_r . They are in series with L_s and R_s . C_m and R_m symbolize the capacitance and resistance of the thin-film between the spiral and insulating layers. C_{mlap} represents the additional overlap capacitance introduced by the magnetic thin-film. R_{mc} represents the ohmic loss due to the eddy current in the thin-film.

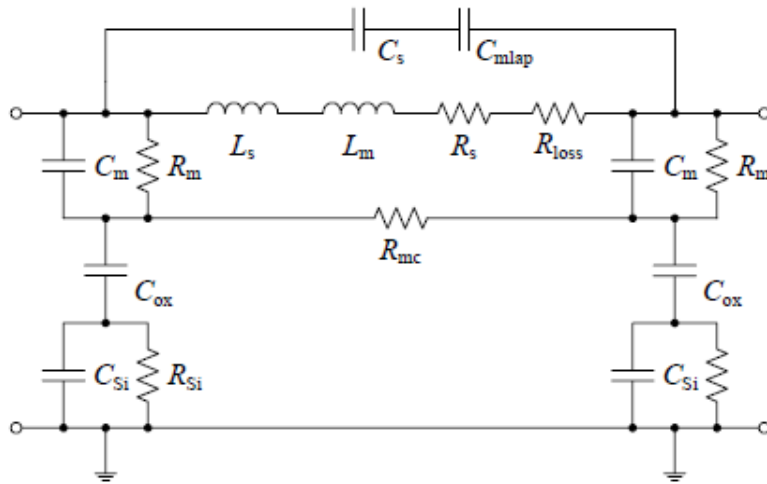


Fig. b Equivalent model of on-chip spiral inductor with magnetic thin film underlayer

For ferrite thin-film, the resistivity is usually above $10^4 \Omega \cdot \text{cm}$, so the eddy current and the ohmic loss in the thin-film are small enough to be neglected. As a result, R_m and R_{mc} are left out as open branches. Then, the model is simplified, as shown in Fig. c, where L_{sm} , R_{sm} , C_{oxm} , C_{sm} are used to substitute the combined impedance of L_s and L_m , R_s and R_m , C_{ox} and C_m , C_s and C_{mlap} , respectively.

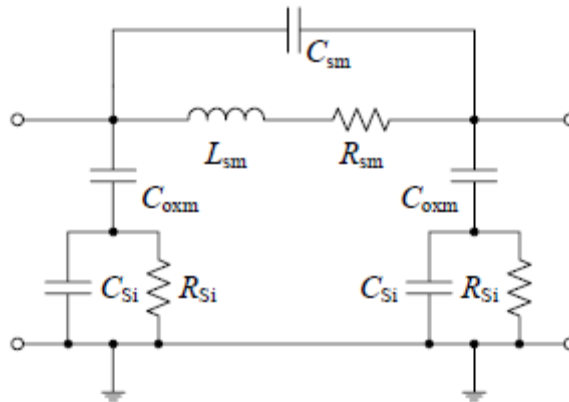


Fig. c Modified equivalent model

Two-port scattering parameters (S -parameters) of the inductors are tested by a vector network analyzer. The as-tested S -parameters are then changed to admittance parameters (Y -parameters), where the system impedance $Z_0 = 50 \Omega$. Using the following equations, the Y -parameters are obtained.

$$S_{11} := S_{11m} \cos(S_{11p}) + j \cdot S_{11m} \sin(S_{11p})$$

m=magnitude

$$S_{12} := S_{12m} \cos(S_{12p}) + j \cdot S_{12m} \sin(S_{12p})$$

p=phase

$$S_{21} := S_{21m} \cos(S_{21p}) + j \cdot S_{21m} \sin(S_{21p})$$

$$S_{22} := S_{22m} \cos(S_{22p}) + j \cdot S_{22m} \sin(S_{22p})$$

$$Z_0 := 50$$

$$D := [(1 + S_{11}) \cdot (1 + S_{22}) - S_{12} \cdot S_{21}]$$

$$y_{11} := \frac{1}{Z_0} \left[\frac{[(1 - S_{11}) \cdot (1 + S_{22}) - S_{12} \cdot S_{21}]}{D} \right]$$

$$y_{12} := -2 \cdot \frac{S_{12}}{D}$$

$$y_{21} := -2 \cdot \frac{S_{12}}{D}$$

$$y_{22} := \left[\frac{[(1 + S_{11}) \cdot (1 - S_{22}) + S_{12} \cdot S_{21}]}{D} \right]$$

$$Y := \begin{pmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{pmatrix}$$

Then, the total inductance L , total resistance R , and Q are extracted according to Y -parameters using the following equations

$$\text{Inductance} := \frac{\text{Im}\left(\frac{1}{y_{11}}\right)}{w}$$

$$Q := \frac{\text{Im}\left(\frac{1}{y_{11}}\right)}{\text{Re}\left(\frac{1}{y_{11}}\right)}$$

$$w := 6.38 \cdot f$$

$$\text{Resistance} := \text{Re}\left(\frac{1}{y_{11}}\right)$$

According to the model in Fig. c, element parameters are extracted. For the inductor with single layer, C_{sm} or C_s in the model only contains the inter-turn capacitance, which is very small. So the C_{sm} and C_s are neglected in parameter extraction. Then the other parameters are extracted as below:

$$L_{sm} := \frac{\text{Im}\left(\frac{-y_{12}}{|Y|}\right)}{w} \quad C_{pm} := \frac{\text{Im}\left(\frac{|Y|}{y_{11}}\right)}{w}$$

$$R_{sm} := \text{Re}\left(\frac{-y_{12}}{|Y|}\right) \quad R_{pm} := \text{Re}\left(\frac{|Y|}{y_{11}}\right)$$

The mutual inductance can be obtained from $L_m = \alpha L_s$ (α is coupling co-efficient)

or $L_m = L - L_{sm}$.

At low frequencies, the electric field mainly exists in the dielectric and is primarily determined by C_{oxm} . Since almost all electric energies are stored within the dielectric layer along the spiral, little conduction current flows into the silicon substrate. Thus, R_{pm} and R_p are large. As frequency increases, the electric field starts to penetrate into the silicon substrate, which reduces C_{oxm} and C_{ox} because of the series connection of oxide and silicon substrate capacitances. The roll-off of R_{pm} and R_p signifies the increasing energy dissipation in the silicon substrate.

L, R, Q and other model values for given S-parameters were obtained, using MATHCAD.

APPENDIX B

Voltage and current requirements for CPU processors and portable devices

Output voltage and current requirements for intel processors [42]

The output voltage requirements vary from 0.83125 V to 1.6 V for a 7 bit VR (voltage regulator)

The output voltage requirements vary from 0.03125 V to 1.6 V (usable range 0.5 V-1.6 V) for a 8 bit VR

The VRM/EVRD 11.0 is required to support the following:

1. Maximum continuous load current (I_{CCTDC}) of 130 A
2. Maximum load current (I_{CCMAX}) of 150 A peak
3. Maximum load current step (I_{CCSTEP}), within a 1 μs period, of 100 A
4. Maximum current slew rate (dI_{CC}/dt) of 1200 A/ μs at the lands of the processor

Portable device requirements

Constraints on buck regulators for battery powered applications include size, efficiency, cost, and load range. A high performance solution is based on a 2 MHz buck converter powered from two Li-ion cells that provide 1.8 V at up to 500 mA.

Some of the converters available in market

	Supply Current	Output Voltage	Efficiency	Frequency
MIC2238 (Micrel)[43]	800 mA	0.8 V	94 ~96 %	2.5 MHz
FAN5350 (Fairchild)[44]	600 mA	1.82 V	90 %	3 MHz
MAX8640Y (Maxim)[45]	500 mA	0.8 V to 2.5 V	---	4 MHz or 2 MHz
The TSP62240, TSP62260 and TSP62290 (Instruments)[46]	300 mA, 600 mA and 1 A	2.5 V or 1.1 V	95 %	---
LTC3560 (Linear Technology)[47]	800mA	2.5 V to 5.5 V	95%	2.25 MHz
EP53x2Q (Enpirion)[48]	500 mA, 600 mA and 800 mA	0.6 ~ ($V_{in} - 0.45$) V		5 MHz

Summarizing the requirements for portable and CPU processors from the DC-DC converters

	Supply Current	Output Voltage	Frequency
CPU Processors	> 50 A	0.8 – 1.6 V	>500 kHz
Portables	300 mA – 1 A	0.8 – 5 V (or close to the supply voltage)	> 1 MHz

APPENDIX C

Theoretical evaluation for output voltage, current and ripple values

Defining values:

$$L1 := 20 \cdot 10^{-9} \quad C1 := 560 \cdot 10^{-6} \quad ts := \frac{1}{f}$$

d = Duty cycle ratio (0.34)

Vin = Input voltage (3.6 V)

L1 = Inductance (H)

C1 = Output capacitance (F)

ts = Time period

f = Frequency of operation

Output voltage:

$$Vo := d \cdot Vin = 1.224$$

Output current:

$$Io := \frac{ts \cdot Vo}{2 \cdot L1} \cdot (1 - d)$$

Ripple voltage

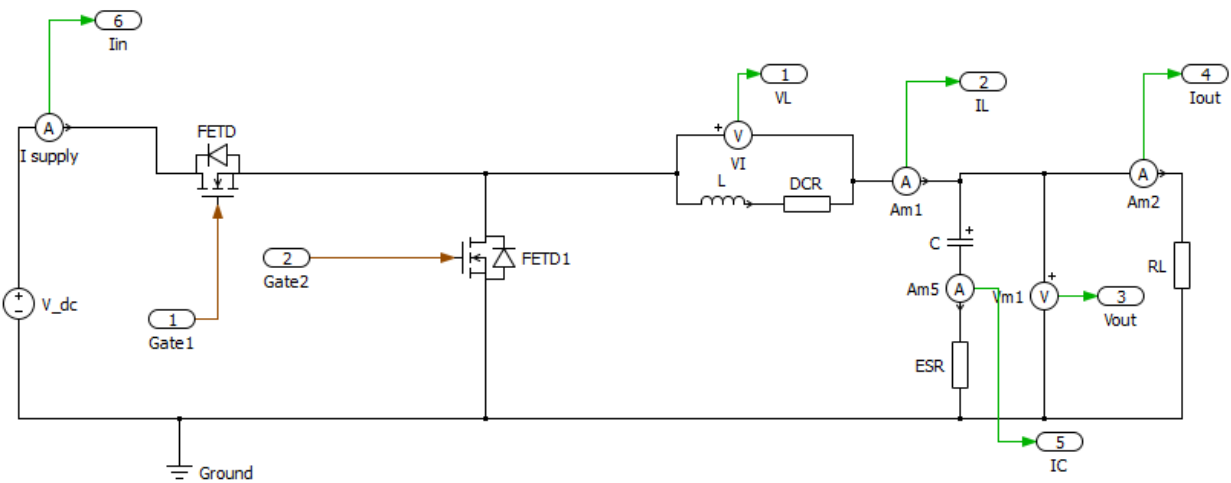
$$\Delta V_o := \frac{t_s \cdot V_o}{8 \cdot C_1 \cdot L_1} \cdot t_s \cdot (1 - d)$$

Calculated Theoretical Values:

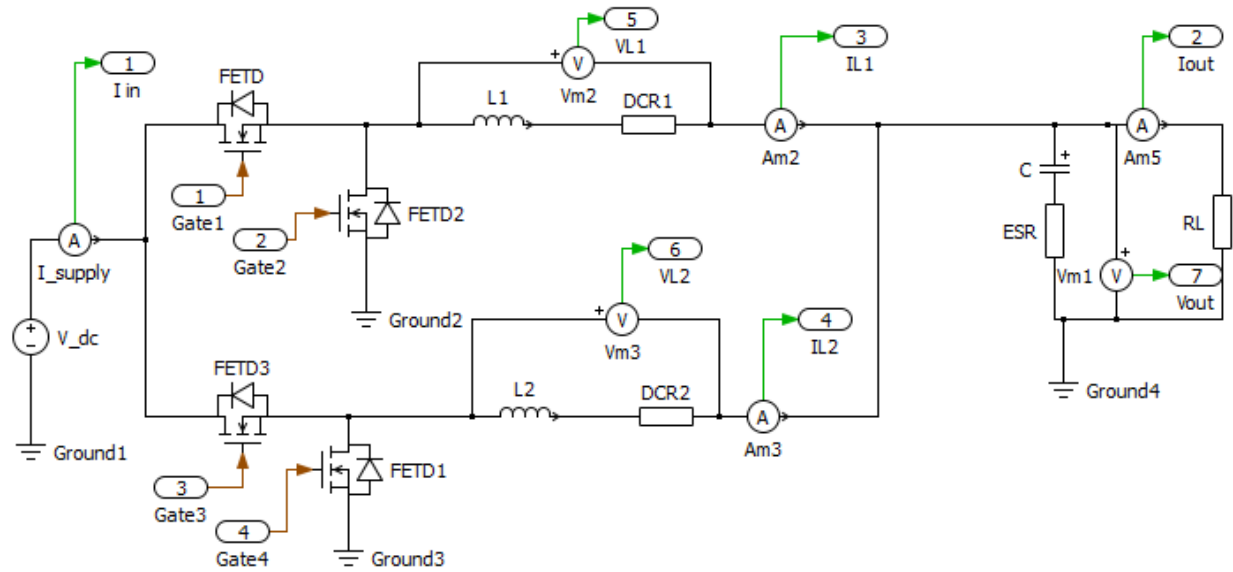
Frequency (MHz)	Output Voltage (V)	Output Current (A)	Output Ripple Voltage (mV)
1	1.224	20.196	9.016
5	1.224	4.039	0.3606
10	1.224	2.02	0.09016

PLECS Circuit

Single-phase



Two-phase



$L, L1, L2$ = Inductors of equal inductance

$DCR, DCR1, DCR2$ = Equivalent DC resistance of the inductors

C = Output capacitance

ESR = Equivalent series resistance of the capacitor

RL = Load resistance

$FETD$ = MOSFET transistors used each having $R_{DS_ON} = 3 \text{ m}\Omega$